M2i.31XX - 8-Channel, up to 25 MS/s, 12 bit, PCI-based Transientrecorders

Features:

- **PCI-X interface (100% compatible to PCI)**
- **Multichannel 12 bit A/D converter board**
- **Up to 25 MS/s on one, two or four channels**
- **Separate ADC and Amplifier per channel**
- **Simultaneous sampling on all channels**
- **8 input ranges: ±50 mV up to ± 10 V**
- **64 MB on-board memory expandable to 4 GB**
- **Sustained streaming mode to 200 MB/s**
- **Window, pulse-width, re-arm, OR/AND trigger**
- **Programmable input offset up-to +/- 100%**
- **Synchronization option for up-to 16 boards**
- **ABA mode option: combination of data logging and digitizing on trigger**
- **Software support for Windows and LINUX**

Description:

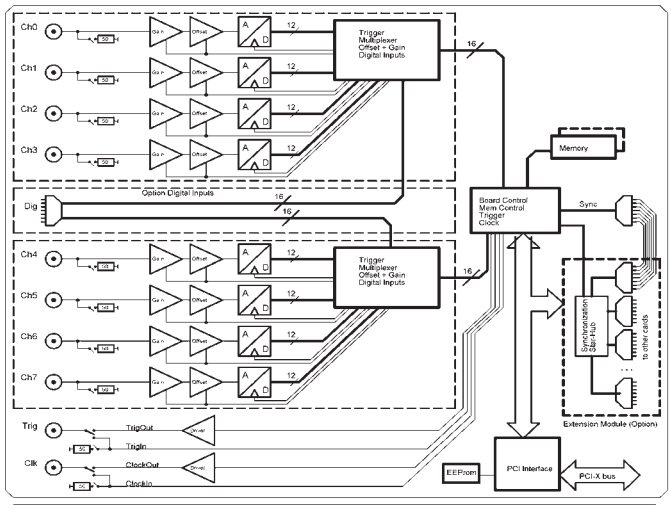
The M2i.31xx series allows recording of two, four or eight channels with sampling rates of 1 MS/s, 10 MS/s or 25 MS/s. Due to the proven design a wide variety of 12 bit A/D converter boards for PCI/PCI-X bus can be offered. These boards are available in several versions and different speed grades making it possible for the user to find an individual solution.As an option 4 digital inputs per channel can be recorded synchronously. The installed memory of up to 2 GSample will be used for fast data recording. It can be used completely by the currently active channels. If using slower sampling rates the memory is switched to a FIFO buffer and data will be transferred on-line to the PC memory or to hard disk.

- Completely new developed base card
- 4 GByte memory with one slot width
- Optimized low jitter clock section
- Multi, Gate with programmable pre, posttrigger and timestamp
- Zero phase delay synchronization
- AND/OR conjunction of trigger/gate

Model	1 channel	2 channels	4 channels	8 channels
M2i.3110	1 MS/s	1 MS/s		
M2i.3111	1 MS/s	1 MS/s	1 MS/s	
M2i.3112	1 MS/s	1 MS/s	1 MS/s	1 MS/s
M2i.3120	10 MS/s	10 MS/s		
M2i.3121	10 MS/s	10 MS/s	10 MS/s	
M2i.3122	10 MS/s	10 MS/s	10 MS/s	10 MS/s
M2i.3130	25 MS/s	25 MS/s		
M2i.3131	25 MS/s	25 MS/s	25 MS/s	
M2i.3132	25 MS/s	25 MS/s	25 MS/s	25 MS/s

Applications:

- **Automation**
- **OEM-Applications**
- **Quality control**
- **Military**
- **Automotive**
- **ATE**



Hardware block diagram

M2i.31xx 23062006

Product range overview

All four cards of the M2i.31xx series may use the whole installed on-board memory completely for the currently activated number of channels. See details above

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Specifications:

RESOLUTION: 12bit
DIFF. NONLINEARITY: ≤ 1 LSB typ. (ADC)
INTEGRAL NONLINEARITY: ≤ 2.5 LSB typ. (ADC)
OFFSET ERROR: can be calibrated by the user
GAIN ERROR: <1% of current value
PROGRAMMABLE INPUT OFFSET: +/-100% of current input range
CROSSTALK @ +50mV, 50 Ohm, 500 kHz: <-70db between any adjacent channel
INPUT SIGNAL with 50 Ohm termination: max. 5V rms
OVER VOLTAGE PROTECTION ≤+/-1V: +/-5V
OVER VOLTAGE PROTECTION ≥+/-1V: +/-50V
CONNECTOR (analog and trigger/clock): 3mm SMB m

MULTI, GATE, re-arming time: <4 Samples
MAX PRETRIGGER at MULTI, GATE; FIFO: 8176 samples as sum of all active channels
CHANNEL TRIGGER RES.:
TRIGGER OUTPUT delay:
EXT.TRIGGER type: TTL compatible
EXT.TRIGGER input: low ≤ 0.8V, high ≥2V, ≥2 clock periods
EXT.TRIGGER max voltage: -0.5V to +5.5V
EXT.TRIGGER output levels: TTL comp.
EXT.TRIGGER output: capable of driving a 50 Ohm load

INTERNAL CLOCK accuracy: 20 ppm
INT. CLOCK RANGE: 1 kS/s to max.
INT. CLOCK max. jitter (PPL mode):
INT. CLOCK max. jitter (Quartz mode):
INT. CLOCK stepsize: ≤1% of range (100M, 10M..)
INT. CLOCK stepsize example: range 1 to 10MMS/s: stepsize ≤ 100k
EXT. CLOCK RANGE: 1 MS/s to max.-see table
EXT. CLOCK DELAY to int. clock:
EXT. CLOCK INPUT: low ≤ 0.8V, high ≥2V, duty 45-55%
EXT. CLOCK max. voltage: -0.5V to +5.5V
EXT. CLOCK output: low ≤0.4V, high ≥2.4V (TTL)
EXT. CLOCK output: capable of driving a 50 Ohm load
REF. CLOCK-EXT.CLOCK RANGE: ≥4 MHz ≤125 MHz

DIGITAL INPUTS input impedance: 110 Ohm @ 2.5V
DIGITAL INPUTS delay to analog sample:
MAXIMUM VOLTAGE: -0.3 to +5.5V
INPUT VOLTAGE: low ≤ 0.8V, high ≥2.0V
CONNECTOR digital inputs: 40 pole half pitch (Hirose FX2 series

DIMENSION: 312 x 107 mm (full lengths PCI board)
With STAR-HUB 5 / 16: 1 / 2 full size slot
With DIG.INPUTS: 1 full size slot + 1/2 size slot
WEIGHT: from 290g to 460g depending on channels and options (w/o packing)

WARMUP TIME: 10 min
OPERATING TEMP RAMGE: 0 to 50 °C
STORAGE TEMP RAMGE: -10 to70 °C
HUMIDITY: 10% to 90%

Please note: The M2i.30x-Series Transientrecorders extensively use SMB connectors. Cables with theses connectors are not included with the boards. They have to be ordered separately if required.

FAST ComTec supports LINUX

Software programmable parameters M2i.31xx		Software programmable parameters M2i.31xx	
Input range	±50 mV to ±10 V in steps of 1, 2, 5	Trigger mode	Channel, External, SW, Auto, Pulse
Input Impedance	50 Ohm / 1 MOhm (relais)		Window, Re-arm, OR/AND, Delay
Input Offset	±100% of input range in steps of 1%	Triggerlevel	TBD
Clock mode	Int. PLL, int. Quartz, ext clock, ext.div. Ext.ref.	Triggeredge	rising edge, falling edge or both edges
	clock, sync	Trigger pulsewidth	0 to /64k-1) samp. in steps of 1 samp.
Clock impedance	50 Ohm / high impedance (>4kOhm)	Trigger delay	0 to /64k-1) samp. in steps of 1 samp.
Trigger impedance	50 Ohm / high impedance (>4kOhm)	Post trigger	4 up to (8G-4) samples in steps of 4
Memory depth	8 up to (installed memory/active channels	Multiple Rec. Seg.	8 up to (installed memory/2/active
	in steps of 4		channels in steps of 4
Channel selection	Any number of channels (see manual for	Multi/Gated pretrigger	0 up to (8k sampl./active chan.-16)
	selections limits)		in increments of 16 samples.
ABA Clock Driver	1 up to (64-1) in steps of 1	Sync. Clock driver	2 up to (8k-2) in steps of 2

Power Consumption (max speed)	3.3 V	5 V	-12 V	+12 V	Total
M2i.31x0 (32 MS memory)					
M2i.31x1 (32 MS memory)					
M2i.31x2 (32 MS memory)					

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Software Support

Windows drivers

The cards are delivered with drivers for Windows 2000, Windows XP, Windows XP64 and Windows Vista (Beta). Programming examples for Visual C/C++, Borland C++ Builder, Gnu C, LabWindows/CVI, Borland Delphi and Visual Basic are included.

Linux Drivers

All cards are delivered with full Linux support. Pre compi-led kernel modules are included for the most common dis-tributions like RedHat, Suse or Debian. The linux support is enhanced by SMP support, versatile programming examples as well as the possibility to get the driver sources for own compilation.

SBench

A full licence of SBench the easy-to-use graphical operating software for the Spectrum cards is included in the delivery. The version 6 is running under Windows as well as under Linux (KDE and GNOME)

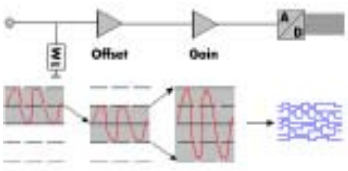
Third-party products

A lot of third-party products are supported as an option. Choose between LabVIEW, MATLAB, DASYLab and Agilent VEE. All drivers come with examples and detailed documentation.

MI Software compatibility layer

To allow an easy change from MI cards to the new M2i cards for existing software a special software compatibility layer is delivered with the cards. This DLL converts MI calls to M2i calls and simulates a MI card in the software.

Hardware features and options

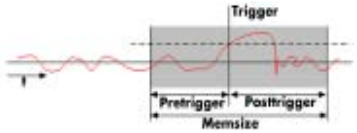


The analog inputs can be adapted to real world signals using a wide variety of settings that are individual for each channel. By using software commands the input termination can be changed between 50 Ohm and 1 MOhm, one can select a matching input range and the signal offset can be compensated for.

Ring buffer mode

Ring buffer mode

The ring buffer mode is the standard mode of all oscillos-cope boards. Data is written in a ring memory of the board until a trigger event is detected. After the event the posttrigger values are recorded. Because of this continuously recording into a ring buffer there are also samples prior to the trigger event visible: Pretrigger = Memsize - Posttrigger.



FIFO mode

The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 225 MB/s on a PCI-X slot and up to 115 MB/s on a PCI slot) or hard disk. The control of the data stream is done automatically by the driver on interrupt request. The complete installed on-board memory is used for buffer data, making the continuous streaming extremely reliable.

Channel trigger

The data acquisition boards offer a wide variety of trigger modes. Besides the standard signal checking for level and edge as known from oscilloscopes it's also possible to define a window trigger. All trigger modes can be combined with the pulsewidth trigger. This makes it possible to trigger on signal errors like too long or too short pulses. In addition to this a re-arming mode (for accurate trigger recognition on noisy signals) the AND/OR conjunction of different trigger events is possible. As a unique feature it is possible to use deactivated channels as trigger sources.

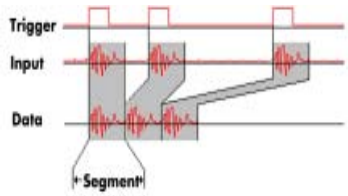
External trigger I/O

All boards can be triggered using an external TTL signal. It's possible to use positive or negative edge also in combination with a programmable pulse width. An internally recognised trigger event can - when activated by software - be routed to the trigger connector to start external instruments.

Pulse width

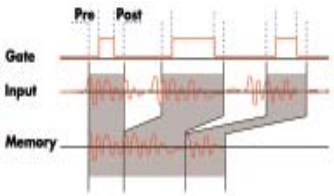
Defines the minimum or maximum width that a trigger pulse must have to generate a trigger event. Pulse width can be combined with channel trigger, pattern trigger and external trigger.

Multiple Recording



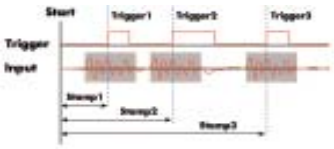
The Multiple Recording option allows the recording of several trigger events with an extremely short re-arming time. The hardware doesn't need to be restarted in between.
The on-board memory is divided into several segments of the same size. Each of them is filled with data if a trigger event occurs. Pre- and posttrigger of the segments can be programmed. The number of acquired segments is only limited by the used memory and is unlimited when using FIFO mode.

Gated Sampling



The Gated Sampling option allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level. In addi-tion a pre-area before start of the gate signal as well as a post area after end of the gate signal can be acquired. The number of gate segments is only limited by the used memory and is unlimited when using FIFO mode.

Timestamp



The timestamp option writes the time positions of the trigger events in an extra memory. The timestamps are relative to the start of recording, a defined zero time, externally synchronised to a radio clock, or a GPS receiver. With this option acquisitions of systems on different locations can be set in a precise time relation.

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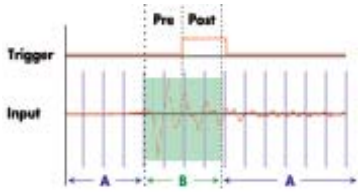
ABA mode



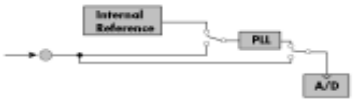
The optional ABA mode combines slow continuous data recording with fast acquisition on trigger events. The ABA mode works like a slow data logger combined with a fast digitizer. The exact position of the trigger events is stored as timestamps in an ex-tra memory.

External clock I/O

Using a dedicated connector a sampling clock can be fed in from an external system. It's also possible to output the internally used sampling clock to synchronise external equipment to this clock.

Reference clock

The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronise the board for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.



Star-Hub

The star-hub is an additional module allowing the phase stable synchronisation of up to 16 boards. Independent of the number of boards there is no phase delay between all channels. The star-hub distributes trigger and clock information between all boards. As a result all connected boards are running with the same clock and the same trigger. All trigger sources can be combined with OR/AND allowing all channels of all cards to be trigger source at the same time. The star-hub is available as 5 card and 16 card version. The 5 card version doesn't need an extra slot.

Dynamic Parameters	M2i.3110 M2i.3111	M2i.3112	M2i.3120 M2i.3121	M2i.3122	M2i.3130 M2i.3131	M2i.3132
Max internal clock	1 MS/s	1 MS/s	10 MS/s	10 MS/s	25 MS/s	25 MS/s
Max external clock	1 MS/s	1 MS/s	10 MS/s	10 MS/s	25 MS/s	25 MS/s
-3 dB bandwidth	DC..0.5 MHz	DC..0.5 MHz	DC..5 MHz	DC..5 MHz	DC..12.5 MHz	DC..12.5 MHz
Zero noise level (<125 MS/s)						
Zero noise level (>125 MS/s)						
Test Srate for SNR, THD, SFDR, ENOB	1 MS/s	1 MS/s	10 MS/s	10 MS/s	25 MS/s	25 MS/s
Test signal frequency	10 /90 kHz	10 /90 kHz	0.09 / 1 MHz	0.09 / 1 MHz	1 / 4 MHz	1 / 4 MHz
SNR typ (dB)						
THD typ. (dB)						
SFDR typ. excl. harmonics (dB)						
ENOB based on SNR (LSB)						
ENOB based on SINAD (LSB)						

Certifications and Compliances: **EMC Immunity and emission:** compliant with CE Mark

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Ordering Information

M2i.31xx-12 bit A/D conv., up to 25 MS/s, up to 8 channels, memory 32 MS (64 MB) , PCI-Bus						
Model					**Description**	**Order No**
	1ch	2ch	4ch	8ch		
M2i.3110	1MS	1MS			Input: ±(50mV ... 10V)	TR3110
M2i.3111	1MS	1MS	1MS		Input: ±(50mV ... 10V)	TR3111
M2i.3112	1MS	1MS	1MS	1MS	Input: ±(50mV ... 10V)	TR3112
M2i.3120	10MS	10MS			Input: ±(50mV ... 10V)	TR3120
M2i.3121	10MS	10MS	10MS		Input: ±(50mV ... 10V)	TR3121
M2i.3122	10MS	10MS	10MS	10MS	Input: ±(50mV ... 10V)	TR3122
M2i.3130	25MS	25MS			Input: ±(50mV ... 10V)	TR3130
M2i.3131	25MS	25MS	25MS		Input: ±(50mV ... 10V)	TR3131
M2i.3132	25MS	25MS	25MS	25MS	Input: ±(50mV ... 10V)	TR3132
Drivers M2i.31x						
M2i.ml					MATLAB driver for all M2i cards	TRml
M2i.31-lv					LabVIEW driver for all M2i.31xx cards	TR31lv
M2i.31-dl					DASYLab driver for all M2i.31xx cards	TR31dl
M2i.31-vee					Agilent VEE driver for all M2i.31xx cards	TR31vee

Memory Expansions M2i.3x, M2i.4x		
Model	**Description**	**Order No**
M2i.64MS	Mem. Exp. to 64 MS (128MB) for M2i.3x and M2i.4x series	TR64MS
M2i.128MS	Mem. Exp. to 128 MS (256MB) for M2i.3x and M2i.4x series	TR128MS
M2i.256MS	Mem. Exp. to 256 MS (512MB) for M2i.3x and M2i.4x series	TR256MS
M2i.512MS	Mem. Exp. to 512 MS (1 GB) for M2i.3x and M2i.4x series	TR512MS
M2i.1GS	Mem. Exp. to 1 GS (2 GB) for M2i.3x and M2i.4x series	TR1GS
M2i.2GS	Mem. Exp. to 2 GS (4 GB) for M2i.3x and M2i.4x series	TR2GS
Options		
M2i.mr	Option Multiple Recording	TRmr
M2i.mgt	Option Multiple Recording, Gated Sampling, Timestamp	TRmgt
M2i.mgtab	Option Multiple Rec., Gated Sampling, Timestamp, ABA Modus	TRmgtab
M2i.SH5 (1)	Synchronisation Star-Hub for up to 5 cards, only 1 slot width	TRSH5 (1)
M2i.SH16 (1)	Synchronisation Star-Hub for up to 16 cards, only 1 slot width	TRSH16 (1)
M2i.bxio	Option BaseXIO: 8 digital I/O lines for asynchronous I/O, timestamp	TRbxio
	ref-clock, addl. Ext.rigger lines, addl bracket with 8 SMB connectors	
Options for M2i.3x		
M2i.3-dig	Additional synchronous digital inputs (4 per analog channel)	TR3dig
	including Cab-d40-idc-100	
Cables for all M2ix boards		
Cab-1m-9m-80	Adapter cable MMCX male to BNC male, 80 cm (for analog inputs)	Cab-1m-9m-80
Cab-1m-9f-80	Adapter cable MMCX male to BNC female, 80 cm (for analog inputs)	Cab-1m-9f-80
Cab-1m-9m-200	Adapter cable MMCX male to BNC male, 200 cm (for analog inputs)	Cab-1m-9m-200
Cab-3f-9m-80	SMB female to BNC male 80cm	Cab-3f-9m-80
Cab-3f-9f-80	SMB female to BNC female 80cm	Cab-3f-9f-80
Cab-3f-3f-80	SMB female to SMB female 80cm	Cab-3f-3f-80
Cab-3f-9m-200	SMB female to BNC male 200cm	Cab-3f-9m-200
Cab-3f-9f-200	SMB female to BNC female 200cm	Cab-3f-9f-200
Cab-3f-3f-200	SMB female to SMB female 200cm	Cab-3f-3f-200
Cab-3f-9f-5	Adapter cable SMB female to BNC female, 5 cm	Cab-3f-9f-5
	(short cable especially for oscilloscope probes)	
Cables for M2i.4x and M2i.3x		
Cab-d40-idc-100	Flat ribbon cable 40 pin FX2 dig. conn. to 2x20 pin IDC conn.100 cm	Cab-d40-idc-100
Cab-d40-d40-99	Flat ribbon cable 40 pin FX2 for digital connector to	Cab-d40-d40-99
	40 pin digital FX2 conn., 100 cm	