M2i.20XX - 50 MS/s to 200 MS/s, 8 bit, PCI-based Transientrecorders

Features:
- PCI-X interface (100% compatible to PCI)
- Up to 200 MS/s on two channel
- Up to 100 MS/s on four channels
- Simultaneous sampling on all channels
- 7 input ranges: ±50 mV up to ± 5 V
- 64 MB on-board memory expandable to 4 GB
- Sustained streaming mode to 200 MB/s
- Window, pulse-width, re-arm, OR/AND trigger
- Programmable input offset up-to +/- 400%
- Synchronization option for up-to 16 boards
- ABA mode option: combination of data logging and fast digitizing on trigger
- Software support for Windows and LINUX

Description:
The four models of the M2i.20xx series are designed for the fast and high quality data acquisition. Each of the up to four input channels has its own A/D converter and its own programmable input amplifier. This allows to record signals on all channels with 8 bit resolution without any phase delay between them. The inputs can be selected to one of seven input ranges by software and can be programmed to compensate for an input offset of ±400% of the input range. The extremely large on-board memory allows long time recording even with highest sampling rates. A FIFO mode is also integrated on the board. This allows the acquisition of data continuously for online processing in the PC or for data storage on hard disk.

Applications:
- Laser Spectroscopy
- OEM-Applications
- Physics research
- Chemical reaction studies
- LDA/PDA
- RADAR/LIDAR/SONAR
- Telecommunications

<table>
<thead>
<tr>
<th>Model</th>
<th>1 channel max speed</th>
<th>2 channels max speed</th>
<th>4 channels max speed</th>
</tr>
</thead>
<tbody>
<tr>
<td>M2i.2020</td>
<td>50 MS/s</td>
<td>50 MS/s</td>
<td>-</td>
</tr>
<tr>
<td>M2i.2021</td>
<td>50 MS/s</td>
<td>50 MS/s</td>
<td>50 MS/s</td>
</tr>
<tr>
<td>M2i.2030</td>
<td>200 MS/s</td>
<td>100 MS/s</td>
<td>100 MS/s</td>
</tr>
<tr>
<td>M2i.2031</td>
<td>200 MS/s</td>
<td>200 MS/s</td>
<td>100 MS/s</td>
</tr>
</tbody>
</table>

Hardware block diagram

Product range overview
All four cards of the M2i.20xx series may use the whole installed on-board memory completely for the currently activated number of channels. See details on next page.
Specifications:

**RESOLUTION:** 8 bit

**DIFF. NONLINEARITY:** \( \leq 0.5 \text{ LSB typ. (ADC)} \)

**INTEGRAL NONLINEARITY:** \( \leq 0.5 \text{ LSB typ. (ADC)} \)

**OFFSET ERROR:** can be calibrated by the user

**GAIN ERROR:** \(<2\% of current value\)

**PROGRAMMABLE INPUT OFFSET:** \(+/-400\% of current input range\)

**CROSSTALK** 1MHz signal, 50 Ohm trm.: \(<-62\text{db between any adjacent channel}\)

**INPUT SIGNAL with 50 Ohm termination:** max. 5V rms

**OVER VOLTAGE PROTECTION** \(\leq +/-.05\text{V}\):

- +5V
- -5V

**OVER VOLTAGE PROTECTION** \(\geq +/-.05\text{V}\):

- +5V
- -5V

**CONNECTOR (analog and trigger/clock)**: 3mm SMB m

**MULTI, GATE, re-arming time:** <4 Samples

**MAX PRETRIGGER at MULTI, GATE; FIFO:** 16352 samples as sum of all active channels

**TRIGGER ACCURACY** \((\leq100 \text{ MS/s})\): 1 Sample int.or ext.

### Dynamic Parameters

<table>
<thead>
<tr>
<th>Dynamic Parameters</th>
<th>M2i.2020</th>
<th>M2i.2021</th>
<th>M2i.2030</th>
<th>M2i.2031</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min internal clock</td>
<td>1 kS/s</td>
<td>1 kS/s</td>
<td>1 kS/s</td>
<td>1 kS/s</td>
</tr>
<tr>
<td>Max internal clock</td>
<td>50 MS/s</td>
<td>200 MS/s</td>
<td>50 MS/s</td>
<td>50 MS/s</td>
</tr>
<tr>
<td>Min external clock</td>
<td>1 kS/s</td>
<td>1 kS/s</td>
<td>1 kS/s</td>
<td>1 kS/s</td>
</tr>
<tr>
<td>Max external clock</td>
<td>50 MS/s</td>
<td>100 MS/s</td>
<td>50 MS/s</td>
<td>100 MS/s</td>
</tr>
<tr>
<td>-3 dB bandwidth</td>
<td>&gt;25 MHz</td>
<td>&gt;90 MHz</td>
<td>&gt;25 MHz</td>
<td>&gt;90 MHz</td>
</tr>
<tr>
<td>Test rate for SNR, THD, SFDR, ENOB</td>
<td>50 MS/s</td>
<td>100 MS/s</td>
<td>50 MS/s</td>
<td>100 MS/s</td>
</tr>
<tr>
<td>Test signal frequency</td>
<td>1 / 4 MHz</td>
<td>1 / 9 MHz</td>
<td>1 / 4 MHz</td>
<td>1 / 9 MHz</td>
</tr>
<tr>
<td>SNR typ (dB)</td>
<td>45 / 44.5 dB</td>
<td>49.5 dB</td>
<td>59 / 57 dB</td>
<td>7.3 / 7.2</td>
</tr>
<tr>
<td>THD fin = 10 MHz, +/-200 mV</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SFDR fin = 10 MHz, +/-200 mV</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ENOB based on SNR (dB)</td>
<td>7.3 / 7.2</td>
<td>7.3 / 7.2</td>
<td>7.3 / 7.2</td>
<td>7.3 / 7.2</td>
</tr>
<tr>
<td>ENOB based on SINAD (dB)</td>
<td>7.1 / 7.0</td>
<td>7.1 / 7.0</td>
<td>7.1 / 7.0</td>
<td>7.1 / 7.0</td>
</tr>
</tbody>
</table>

### Power Consumption (max speed)

<table>
<thead>
<tr>
<th>Power Consumption (max speed)</th>
<th>3.3 V</th>
<th>5 V</th>
<th>-12 V</th>
<th>+12 V</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>M2i.20x0 (64 MS memory)</td>
<td>2.2 A</td>
<td>0.5 A</td>
<td>n.u.</td>
<td>n.u.</td>
<td>9.8 W</td>
</tr>
<tr>
<td>M2i.20x1 (64 MS memory)</td>
<td>2.8 A</td>
<td>0.8 A</td>
<td>n.u.</td>
<td>n.u.</td>
<td>13.3 W</td>
</tr>
<tr>
<td>M2i.2031 (4 GS memory), max. power</td>
<td>3.9 A</td>
<td>0.8 A</td>
<td>n.u.</td>
<td>n.u.</td>
<td>16.9 W</td>
</tr>
</tbody>
</table>

**TRIGGER ACCURACY** \((\geq100 \text{ MS/s})\): 1 Sample int.or ext. trigger mode

**CHANNEL TRIGGER RES.:** 8 bit

**TRIGGER OUTPUT delay:** 1 positive edge after internal trigger event

**EXT. TRIGGER Accuracy 2/4 channel mode:** 1 Sample

**EXT. TRIGGER type:** TTL compatible

**EXT. TRIGGER input:** low \(\leq 0.8 \text{V}, \text{high } \geq 2 \text{V}, \geq 2 \) clock periods

**EXT. TRIGGER max voltage:** -0.5V to +5.5V

**EXT. TRIGGER output levels:** TTL comp.

**EXT. TRIGGER output:** capable of driving a 50 Ohm load

**INTERNAL CLOCK** 20 ppm

**DIMENSION:** 312 x 107 mm (full lengths PCI board)

**WEIGHT:** from 290g to 420g depending on channels and options (w/o packing)

**WARMUP TIME:** 10 min

**OPERATING TEMP RANGE:** 0 to 50 °C

**STORAGE TEMP RANGE:** -10 to 70 °C

**HUMIDITY:** 10% to 90%

**Please note:** The M2i.20x-Series Transient Recorder extensively use SMB connectors. Cables with these connectors are not included with the boards. They have to be ordered separately if required.
Pretrigger = Memsize - Posttrigger.

a ring buffer there are also samples prior to the trigger event visible:
stream is done automatically by the driver on interrupt request. The
and up to 115 MB/s on a PCI slot) or hard disk. The control of the data
measurement board and PC memory (up to 225 MB/s on a PCI-X slot
The FIFO mode is designed for continuous data transfer between
between 50 Ohm and 1 MOhm, one can select a matching input range and the signal
offset can be compensated for.

Ring buffer mode
The ring buffer mode is the standard mode of all oscilloscope
boards. Data is written in a ring memory of the board until a trigger event is
detected. After the event the postrigger values are recorded. Because of this
continuously recording into a ring buffer there are also samples prior to the trigger event visible: Pretrigger = Memsize - Postrigger.

FIFO mode
The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 225 MB/s on a PCI-X slot and up to 115 MB/s on a PCI slot) or hard disk. The control of the data stream is done automatically by the driver on interrupt request. The complete installed on-board memory is used for buffer data, making the continuous streaming extremely reliable.

Channel trigger
The data acquisition boards offer a wide variety of trigger modes. Besides the standard signal checking for level and edge as known from oscilloscopes it’s also possible to define a window trigger. All trigger modes can be combined with the pulselength trigger. This makes it possible to trigger on signal errors like too long or too short pulses. In addition to this a re-arming mode (for accurate trigger recognition on noisy signals) the AND/OR conjunction of different trigger events is possible. As a unique feature it is possible to use deactivated channels as trigger sources.

External trigger I/O
All boards can be triggered using an external TTL signal. It’s possible to use positive or negative edge also in combination with a programmable pulse width. An internally recognised trigger event can - when activated by software - be routed to the trigger connector to start external instruments.

Pulse width
Defines the minimum or maximum width that a trigger pulse must have to generate a trigger event. Pulse width can be combined with channel trigger, pattern trigger and external trigger.

Multiple Recording
The Multiple Recording option allows the recording of several trigger events with an extremely short re-arming time. The hardware doesn’t need to be restarted in between. The on-board memory is divided into several segments of the same size. Each of them is filled with data if a trigger event occurs. Pre- and postrigger of the segments can be programmed. The number of acquired segments is only limited by the used memory and is unlimited when using FIFO mode.

Gated Sampling
The Gated Sampling option allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level. In addition a pre-area before start of the gate signal as well as a post area after end of the gate signal can be acquired. The number of gate segments is only limited by the used memory and is unlimited when using FIFO mode.

Timestamp
The timestamp option writes the time positions of the trigger events in an extra memory. The timestamps are relative to the start of recording, a defined zero time, externally synchronised to a radio clock, or a GPS receiver. With this option acquisitions of systems on different locations can be set in a precise time relation.
ABA mode

The optional ABA mode combines slow continuous data recording with fast acquisition on trigger events. The ABA mode works like a slow data logger combined with a fast digitizer. The exact position of the trigger events is stored as timestamps in an extra memory.

External clock I/O

Using a dedicated connector a sampling clock can be fed in from an external system. It’s also possible to output the internally used sampling clock to synchronise external equipment to this clock.

Reference clock

The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronise the board for high-quality measurements with external equipment (like a signal source). It’s also possible to enhance the quality of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

Star-Hub

The star-hub is an additional module allowing the phase stable synchronisation of up to 16 boards. Independent of the number of boards there is no phase delay between all channels. The star-hub distributes trigger and clock information between all boards. As a result all connected boards are running with the same clock and the same trigger. All trigger sources can be combined with OR/AND allowing all channels of all cards to be trigger source at the same time. The star-hub is available as 5 card and 16 card version. The 5 card version doesn’t need an extra slot.
### Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
<th>Order No</th>
</tr>
</thead>
<tbody>
<tr>
<td>M2i.20xx</td>
<td>8 bit transient recorder, up to 200 MS/s onboard memory 64 MB, PCI-Bus</td>
<td></td>
</tr>
<tr>
<td>Model</td>
<td>1ch</td>
<td>2ch</td>
</tr>
<tr>
<td>M2i.2020</td>
<td>50 MS</td>
<td>50 MS</td>
</tr>
<tr>
<td>M2i.2021</td>
<td>50 MS</td>
<td>50 MS</td>
</tr>
<tr>
<td>M2i.2030</td>
<td>200 MS</td>
<td>100 MS</td>
</tr>
<tr>
<td>M2i.2031</td>
<td>200 MS</td>
<td>200 MS</td>
</tr>
</tbody>
</table>

### Drivers for M2i.20x

- **M2i.-ml**: MATLAB driver for all M2i cards (TRml)
- **M2i.20-lv**: LabVIEW driver for all M2i.20xx cards (TR20lv)
- **M2i.20-dl**: DASYLab driver for all M2i.20xx cards (TR20dl)
- **M2i.20-vee**: Agilent VEE driver for all M2i.20xx cards (TR20vee)

### Memory Expansions for M2i.20x

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
<th>Order No</th>
</tr>
</thead>
<tbody>
<tr>
<td>M2i.128MB</td>
<td>Mem. Exp. to 128 MB for M2i.2x series</td>
<td>TR128MB</td>
</tr>
<tr>
<td>M2i.256MB</td>
<td>Mem. Exp. to 256 MB for M2i.2x series</td>
<td>TR256MB</td>
</tr>
<tr>
<td>M2i.512MB</td>
<td>Mem. Exp. to 512 MB for M2i.2x series</td>
<td>TR512MB</td>
</tr>
<tr>
<td>M2i.1GB</td>
<td>Mem. Exp. to 1 GB for M2i.2x series</td>
<td>TR1GB</td>
</tr>
<tr>
<td>M2i.2GB</td>
<td>Mem. Exp. to 2 GB for M2i.2x series</td>
<td>TR2GB</td>
</tr>
<tr>
<td>M2i.4GB</td>
<td>Mem. Exp. to 4 GB for M2i.2x series</td>
<td>TR4GB</td>
</tr>
</tbody>
</table>

### Options

- **M2i.mr**: Option Multiple Recording (TRmr)
- **M2i.mgt**: Option Multiple Recording, Gated Sampling, Timestamp (TRmgt)
- **M2i.SH5 (1)**: Synchronisation Star-Hub for up to 5 cards, only 1 slot width (TRSH5 (1))
- **M2i.SH16 (1)**: Synchronisation Star-Hub for up to 16 cards, only 1 slot width (TRSH16 (1))
- **M2i.bxio**: Option BaseXIO: 8 digital asynchronous I/O, timestamp ref-clock (TRbxio) and add. Ext. trigger lines, add. bracket with 8 SMB connectors

### Cables for all M2ix boards

- **Cab-1m-9m-80**: Adapter cable MMCX male to BNC male, 80 cm (for analog inputs) (Cab-1m-9m-80)
- **Cab-1m-9f-80**: Adapter cable MMCX male to BNC female, 80 cm (for analog inputs) (Cab-1m-9f-80)
- **Cab-1m-9m-200**: Adapter cable MMCX male to BNC male, 200 cm (for analog inputs) (Cab-1m-9m-200)
- **Cab-3f-9m-80**: SMB female to BNC male 80 cm (Cab-3f-9m-80)
- **Cab-3f-9f-80**: SMB female to BNC female 80 cm (Cab-3f-9f-80)
- **Cab-3f-3f-80**: SMB female to SMB female 80 cm (Cab-3f-3f-80)
- **Cab-3f-9m-200**: SMB female to BNC male 200 cm (Cab-3f-9m-200)
- **Cab-3f-9f-200**: SMB female to BNC female 200 cm (Cab-3f-9f-200)
- **Cab-3f-3f-200**: SMB female to SMB female 200 cm (Cab-3f-3f-200)
- **Cab-3f-9f-5**: Adapter cable SMB female to BNC female, 5 cm (short cable especially for oscilloscope probes) (Cab-3f-9f-5)