Quint Constant Fraction Trigger 2155
(Pent CFT)

Short Instruction Manual

Version 1.0, 04.08.2017

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1. Introduction

1.1 General description

The Pent CFD is a five-fold fully dc-coupled constant fraction discriminator with a dynamic range of up to 500:1. Selected fraction and three operating modes provide optimum time resolution for many detector types and applications.

The unit accepts negative polarity pulses to the 50Ω terminated dc-coupled inputs. For positive polarity input pulses see section 6. The constant fraction composite signal is formed by the sum of a direct, attenuated (fraction f) signal path and a delayed, unattenuated path. The delay time is selectable according to the propagation delay of a (external) 50Ω BNC cable. Careful selection of fraction and delay cable provides full compensation of timing distortions due to both amplitude and rise time variations in the input signal. Output signals are generated whenever the input signal exceeds the selected threshold set by a front panel potentiometer (T).
Four simultaneous, independent output signals are provided. The two positive NIM voltage outputs (at the rear panel) are adjustable (internal trim potentiometer) in width from 5 ns to 200 ns. The two independent negative NIM current outputs are derived as fixed width pulses (see also section 3 and 4).
The wide dynamic range of the pent CFD permits its use in many timing applications without the need of fast pulse amplifiers.

1.2 Setup information

1.2.1 Selection of modes

CFT	constant fraction discriminator Jumper J2 is set
CFR	constant fraction discriminator with slow rise time reject, no jumpers are set
LET	leading edge trigger, both jumpers are set

1.2.2 Fraction

The factory set fraction is f = 0.4. If a different fraction is required, the resistors R1 and R2 have to be modified as follows:

$$Z_0 = 50\Omega$$
$$R_1 = Z_0 \cdot f$$
$$R_2 = Z_0 / f$$

2. Specifications

2.1 Inputs

Input proceeds -10mV to about -3.5V linear pulses (ref. to common mode range of ultra fast comparators); rise time ≥ 700ps typically; Z_{in} = 50Ω; dc-coupled, front panel Lemo connector; minimum input width ≥ 1 ns; in the LET mode the unit accepts shorter input pulses.

Delay two LEMO connectors for an external delay cable in order to form the internal constant fraction signal.
For specific length see section 4.2.3.

2.2 Outputs

Inspect **M** displays output signal of zero crossing discriminator for use in trimming the time walk.

Neg output two independent negative current outputs, each providing -32 mA into 50Ω, rise time ≈ 2 ns, pulsewidth ≤ 5 ns nominal.

Pos output two independent positive voltage outputs at the rear panel, providing 2 V into 50Ω, rise time ≈ 4 ns, width adjustable by circuit board trimming potentiometer (**W**). The width can be adjusted from about 5 ns to 200ns. Larger width is possible by changing capacitor C4.

2.3 Controls

Threshold **T** front panel (screwdriver) potentiometer to set acceptance level for input pulses (range ≈ -10 mV to -1 V). The threshold voltage can be measured at the test point **T** on the printed board.

Walk adjust **Z** front panel trimming potentiometer (screwdriver) to compensate walk of the internal zero crossing discriminator

Leading edge width **L** width of the leading edge signal is internally set to 20 ns.
(see test point **L** on the printed board). If adjustable width is wanted a circuit trimming potentiometer (10kOhm) can be inserted.

2.4 Performance

Dynamic range	**5**00 : 1 (regarding the linearity of the input pulses)
Walk (CFT mode)	in CFT mode for a 1 ns rise time input pulse over a 100:1 dynamic range (reference – 2.5 V) ≈ 60 ps: typically ± 30 ps
Count rate	up to ≥ 50 MHz, limited by dead time
Pulse pair resolution	less than 10 ns, or as limited by dead time
Threshold stability	better than ± 0.02% / ^{0}C (± 200 ppm / ^{0}C)
Threshold linearity	± 25 % integral
Temperature range	0 ^{0}C to + 50 ^{0}C

2.5 Delay cable

Typical lengths	for fast pulses ≈ 0.25 m to 0.5 m for pulses from slow detectors (e.g. germanium detectors) for a better determination of the cable length see also section 4.2.3

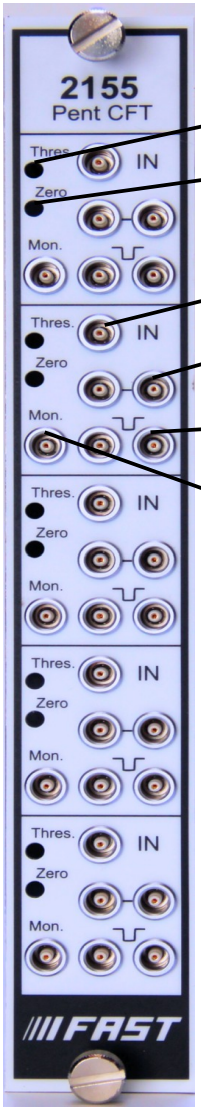
2.6 Power requirements +6.0V / 0.5A ; -6.0V / -1.7A

2.7 Physical

Size	single width 1/12 NIM module (3.43 x 22.13 cm; 1.35 x 8.71 inches) per TID – 20893 (rev.)
Net weight	0.9 kg (2.0 lbs)
Gross weight	1.6 kg (3.0 lbs)

3. Controls and connectors

3.1 Front panel



Threshold setting (-10mV... -1V)

Walk adjust of internal zero crossing detector

Input: -10mV … -3,5V (50 Ohm)

Delay line connectors
(for external 50 Ohm cable)

FAST NIM output (dual)
32mV into 50 Ohm (1,6V neg.)

Monitor output
(Inspect for zero crossing)

3.2 Rear panel

two Lemo connectors for the positive output signals (optional) of each channel A, B, C,D and E. The width of the positive output signal can be set internally (see section 2.2).

4. Operation

4.1 General

The purpose of this section is to familiarize the user with the operation of the pent CFD and to prove that the unit is working properly. The module can be operated in many different system configurations, therefore it is difficult to give explicit operating instructions. However, if the guide line of the listed procedures is followed, the experimentalist will gain sufficient experience with this unit in order to use it properly.

4.2 Laboratory bench tests

Basic performance tests of the unit may be exercised either in a rack mounted NIM-BIN power supply or on a laboratory bench with the unit powered by an extender cable from a NIM-BIN (TID-20893). It is recommended that electrical connections be made with BIN power off. In a laboratory bench it is easy to measure/adjust threshold voltages, width of the leading edge and the positive output signals.

4.2.1 Input

Suitable driving pulses may be obtained from laboratory pulsers or pulse generators, or readily available detector pulse signals. The input network is protected for pulses exceeding 5 V in amplitude. But the user should keep in mind that the linearity is limited by the common mode range of the ultra fast comparators in the input stages.

4.2.2 Operating mode

The selection of the operating mode depends on the requirements of the experiment.

In the **CF** mode (normal constant fraction) the timing is derived from a comparison between an attenuated pulse (fraction f = 0.4; factory set; f can be changed) and a delayed pulse (delay time t_d; external delay cable). The derived time mark is (theoretically) independent of the pulse height of the input signal. For a detailed description of the principle see e.g.:

D.A. Gedcke and W.J. McDonald, Nucl. Instr.& Meth. 56(1968)253

M.R. Maier and P. Sperr, Nucl. Instr. & Meth. 87(1970)13

The choice of the fraction f and the time t_d (see also section 4.2.3) depends on the detector and the experimental setup.

In the **CFRR** mode (constant fraction with slow rise time reject) an option is provided to handle longer rise times (e.g. solid state Ge-detectors). Normally the timing mark for the CF is derived with the presumption that the threshold level has been set quite low and this level is exceeded prior to to the derivation of the

time mark. In the case of long varying wavefronts of the input pulses (and if relatively short delay cables are used) the timing conditions as given above may not be valid. In that case the level discriminator may switch late. The resulting timing mark will represent some mixture of the intended CF timing with leading edge timing. This effect causes tails or even a satellite peak in the time spectrum. In the CFRR mode an option is given which rejects pulses which have not exceeded the threshold level prior to the derived CF timing mark. Some loss in the count rate is obvious.

In the **LET** mode the unit can be used as a simple leading edge trigger up to very high count rates. The leading edge mode should only be used with signals having a very short rise time and a very limited range of amplitudes as change in amplitude will cause walk.

4.2.3 Delay cable

Normally the delay cable used should provide a delay less than the rise time t_r of the input pulses. Theoretically the total delay required can be estimated from the following relation:

$t_d \approx (1 - f) \cdot t_r$ (f = fraction; t_r = rise time of the input signal; t_d = total delay)

it was found to be the optimum for most applications. For very fast pulses it is recommended to measure the delay direct at the input of the high speed comparator (pin 2 and pin 3) and if necessary to directly install a delay cable omitting the front panel connectors.
The delay for suitable cables is ≈ 1.46 ns per foot or ≈ 4.8 ns per meter.

4.2.4 Walk trim

The adjustment of the amplitude sensitive variation of the timing mark (time walk) has to be carried out very carefully (in the CF and the CFRR mode).
Proper adjustment is only possible when the dc-offset present at the input is very small. Thus detector leakage or dark current errors must be minimized before attempting adjustment.
Laboratory trimming of the unit using a fast pulse generator for the first test measurements is recommended. Differenet settings of the walk adjust potentiometer should be tried in order to find the optimum time resolution. When the unit is used with the intended device, time resolution has to be trimmed experimentally by successive measurements with the setup at hand, because the resolution depends on many parameters such as fraction, threshold, delay t_d and walk trim. A quantitative control is available by monitoring the front panel inspect output with an oscilloscope, externally triggered with the fast output of the unit.

For fast detectors it turned out that in most cases the inspect signal (not to be terminated with 50Ω) should go from – 0.4 V to – 0.2 V. (walk trim is already

factory set as described). For slower detectors, a noise band between the levels may be seen, with transitions to high and low of about equal intensity. Symmetrical center setting should be avoided as the ultra fast comparators deviate from their optimum performance in this setting.

4.2.5 Outputs

The output pulses are intended to drive 50Ω loads through any reasonable length of suitable 50Ω coaxial cable (such as RG-58).

5. Circuit description

5.1 General

The pent CFD provides the advantage that various modes of operation (CFT, CFRR, LET) can be chosen. This model utilizes a direct coupled negative input to perform integral discrimination or/and to derive a constant fraction timing mark. The bulk of the logic signal processing is executed in emitter-coupled fast integrated circuit logic (ECL). Reference diodes are used to pin all threshold voltages.

5.1 LET mode

Since the model can be operated in various modes, its operation is best appreciated by understanding the simple LET mode. The input signal is split in a network to serve the two identical ultra fast comparators (IC1 and IC2, see figure). In the LET mode, both pulse amplitude discrimination and timing are derived in the comparator IC1. The pulse acceptance level is established by the front panel threshold potentiometer from -10 mV to – 1.0 V dc. Since the timing mark for the comparator is derived from the point where the pulse intercepts the threshold setting, it is quite obvious that the timing mark changes with amplitude and rise time of the input pulse. The output signal of the comparator (IC1) is accepted through gate IC3 (1/4 of a 10H102) appearing at the outputs as positive going signal (- 1.7 V to – 0.8 V) and as negative going signal (- 0.8 V to - 1.7 V). The width of these signals depends on the setting of the resistor Rv (see circuit layout).

The width can be monitored at the internal test point L. The negative output signal of IC3 is accepted through the gate IC6. Note that with the LET mode (front panel switch) the outputs of the gates IC4 and IC5 are always set to logic LOW (- 1.7 V). The output of gate IC6 is fed to the clock input of a master-slave type D flip-flop IC7 (1/2 of 10H131). The Q – output is fed to a bus driver (10192) and converting the ECL levels to fast NIM levels (- 32 mA in 50Ω). The width of

the output pulse is determined by a RC combination. The output of IC7 goes to the clock enable input of a second master-slave flip-flop IC8 (second half of the 10H131). The output of IC8 is converted by the following ECL – to – TTL translator (10H125) to positive TTL output pulses. The width (min aans, max bbns) of the positive output signal is set internally by a trimmng potentiometer.

5.2 CFT and CFRR mode

In the normal constant fraction mode the applied input signal is sensed for the amplitude by IC1 as described above, but also routed to the front panel DELAY cable BNC connectors. The delayed pulse is applied to the inverting input of the comparator IC2. The non delayed but attenuated signal is applied to the non-inverting input of IC2. The attenuation is determined by the fraction module. The difference signal between these inputs is a bipolar signal whose zero crossing is the time mark. Theoretically the time mark for the bipolar signal is zero. Finite errors, such as small dc-offsets on the input signal, the offset bias of the comparator, as well as the finite gain bandwidth of the device can cause some time shift or walk in the normal case. With the front panel walk adjust (**Z),** by monitoring the inspect signal (**M**) one has the possibility to minimise the time walk. The optimum setting has to be found experimentally. One logic output of IC2 is applied to gate IC5. Jumper J2 is set in CFT operation. The outputs of IC3 and IC5 are applied to gate IC6. In normal operation the first negative going pulse is provided from IC3. The following pulse logic is identical as described above. In the CFT operation jumper J2 is set, the level at the D-input of the flip-flop (IC7) is always logic low (-1.7 V).

In cases where slower rise time pulses may cause poor timing perfomance, the CFRR mode locks out and rejects those pulses which do not satisfy the threshold setting prior to the derived constant fraction timing mark.

In the CFRR mode jumper J2 is not set. The output signal of IC3 is processed through IC4 and applied to the data input of the flip-flop IC7. Therefore output signals are only generated when the threshold signal is prior to the derived timing mark of IC2. Inadvertent timing marks derived from the leading edge discriminator switching late are blocked.

6. Special features and options

In this section some special features of the unit which are available on request are listed.

6.1 Power supply

Normally ± 6 V from a standard NIM BIN, or on customer request, ± 12 V from a NIM BIN. Or on customer request, 220 V (ac)/110 V (ac) independent from a NIM BIN. In this case the unit is mounted in a special housing, for details the supplier should be contacted.

6.2 Input polarity

The standard version of the model 2155 requires negative input polarity. In some cases the output pulses of detectors have positive polarity. If signal transformers (e.g. Ortec IT 100) are not suitable, the module can be modified on customer request to accept positive input signals.

6.3 Output width

As already stated above the unit is available with a fixed output width for the negative output. On customer request the width of the negative output can be enlarged within meaningful values regarding internal settings.

6.4 Threshold

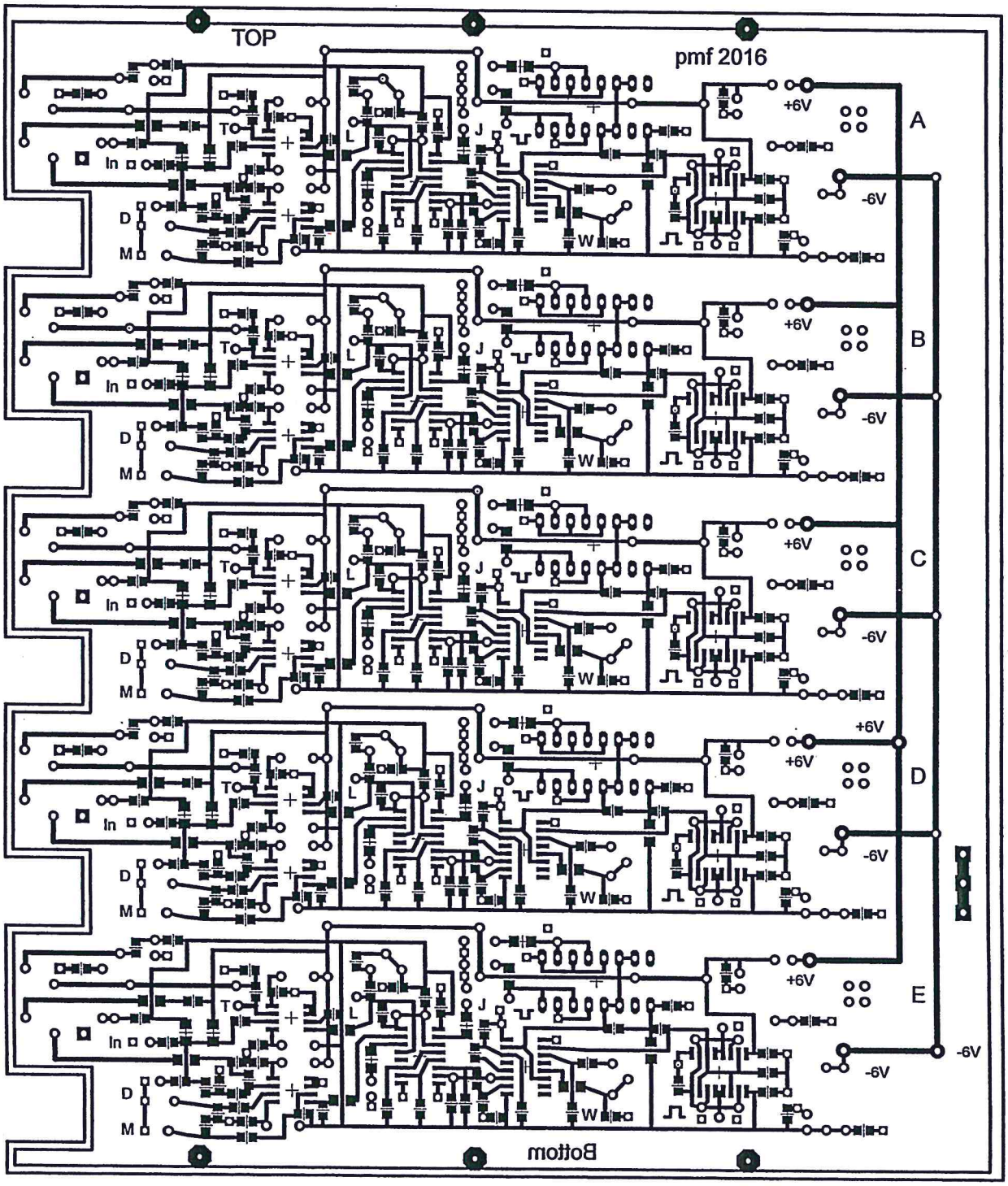
In the standard version the threshold setting is performed via a front panel potentiometer. On customer request the threshold voltage can also be supplied externally (e.g. computer controlled).

6.5 Signal shaping

For some detector systems considerable improvements in time resolution can be achieved using small fractions ($f \approx 0.1$) and “RC-shaping” of the input signal or the attenuated signal (examples are given in the literature). The capacitors (to ground) for the signal shaping (input or attenuated signal) may be implemented. If the capacitor is set at the attenuated signal the delay time t_d has to be adjusted as follows

$$t_d \approx Z_0 \cdot C + (1\text{-}f) \cdot t_r$$

The best values for the fraction f, the capacitor C and the delay t_d have to be determined experimentally.


TOP
pmf 2016
+6V
-6V
A
B
C
D
E
In
D
M
T
L
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