

# 7072T

## Dual Timing 500ns ADC

### User Manual

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The information in this manual describes the hardware and the software as accurately as possible, but is subject to change without notice.

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### 1. Introduction

The Model 7072T is a unique dual channel device that can operate either as an ultra fast pulse height analyzing analog-to-digital converter (PHA ADC) with a fixed conversion time of 500 ns, a time-to-digital converter (TDC) or a sampling voltage analyzer (SVA ADC). The 7072T is ideally suited for high counting rate applications in Energy and Time Spectroscopy. The combined ADC / TDC function finds applications in time resolved photon-, ion-, neutron- and X-ray imaging. The built-in Single Channel Analyzer (SCA) has a separate output on the front panel. This output can be used in the ADC modes in such applications as Moessbauer Spectroscopy. The same connector is used as analog output for monitoring the TAC (Time-to-Amplitude Converter) in TDC mode and four different threshold levels when they are set in the ADJUST mode. In the SVA mode a voltage level or waveform can be sampled when a GATE signal is applied.

The 7072T can be used in any NIM-BIN that supplies  $\pm 6$ ,  $\pm 12$  and  $\pm 24$  V with sufficient power (ref. chapter 4.1.3).

Ample airflow must be provided for sufficient cooling. Do not cover the top or bottom of the NIM-BIN.

## 2. Hardware Description

### 2.1. Overview

The Model 7072T is a single width NIM module. It has two fully equal and independent channels. Both channels are controlled using the front panel buttons and switches. No jumper or switch inside is necessary.

### 2.2. Front panel

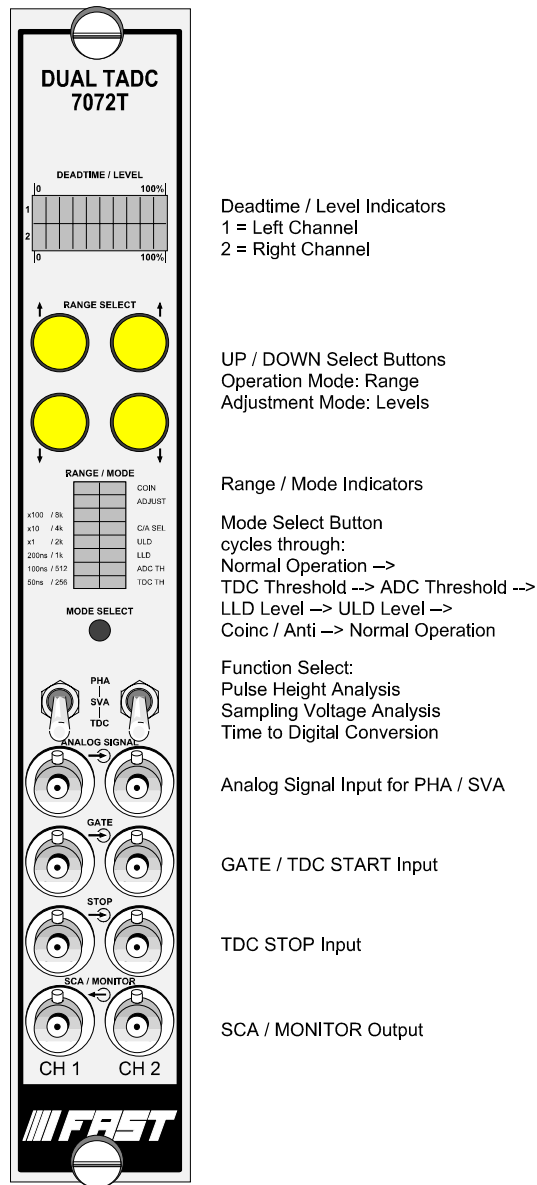


Figure 2.1: Front panel

### 2.2.1. Inputs

#### Signal inputs:

Two BNC connectors accept +25 mV to +10 V (standard / +8 V optional) positive unipolar (positive lobe leading) pulses or a varying voltage level when used in SVA mode. Input impedance = 1 k $\Omega$ , optimized for gaussian shaped pulses with shaping times ranging from 250 ns to 25  $\mu$ s, dc coupled.

#### Gate/Start inputs:

Two BNC connectors accept different signal standards depending on the operating mode.

PHA, SVA mode: accept positive TTL as Gate signals (input impedance = 4.7 k $\Omega$ , pull-up in coincidence and pull-down in anti coincidence). Due to the corresponding change from pull-up to pull-down and vice versa PHA analysis does not require any gate input signal connected.

TDC mode: accept fast NIM pulses as Start signal (input impedance = 50  $\Omega$ ).

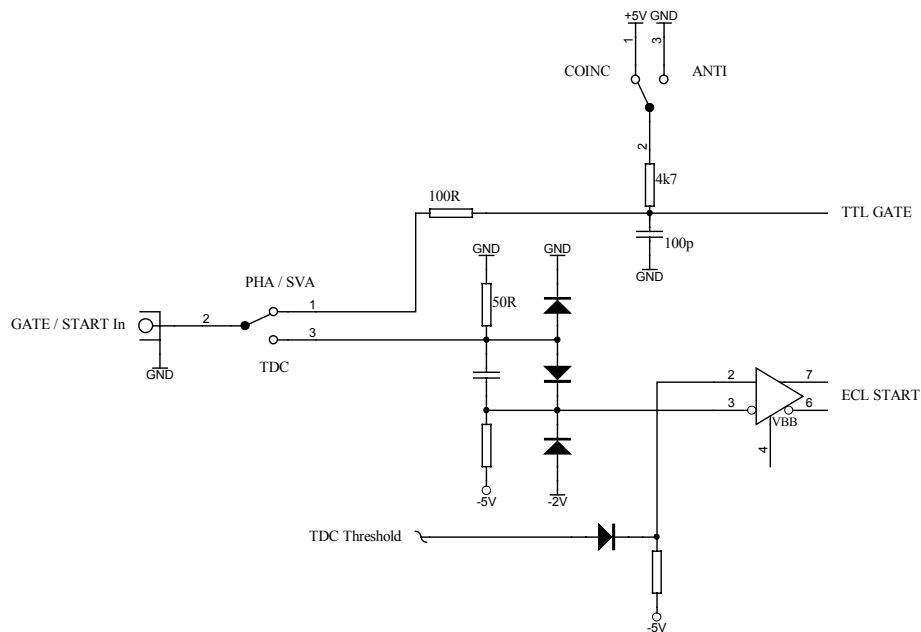
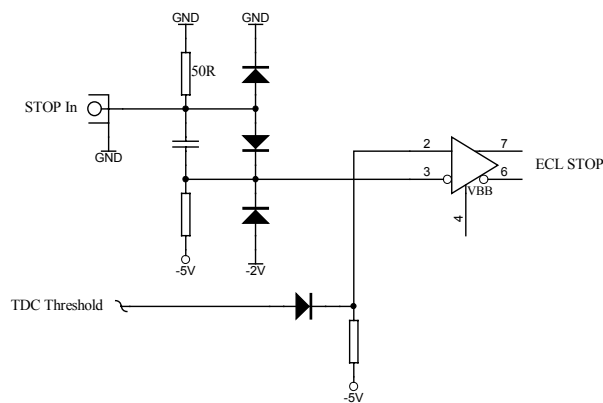


Figure 2.2: Gate/Start input schematic

**Stop inputs:**

Two BNC connectors accept FAST NIM pulses (Stop signals) (input impedance = 50 Ω) in TDC mode. Is not used in PHA/SVA mode.

All FAST-NIM inputs have ECL differential receivers and input diodes as it is shown in Figure 2.3. The diodes are used to prevent the inputs from positive and large negative pulses. The input threshold of the receivers is fine tunable in a range of  $-1.0\text{ V} \dots -0.1\text{ V}$  (referred to the input signal) in steps of 1.22 mV.



**Figure 2.3: FAST-NIM input schematic**

**2.2.2. MONITOR outputs**

Two BNC connectors.

Mode	Function	Output
Operation	PHA	SCA (Single Channel Analyzer) TTL out
	SVA	Not used
	TDC	TAC (Time proportional amplitude)
Adjustment	TDC Threshold	fast NIM threshold level
	ADC Threshold	ADC threshold level
	LLD	Lower level discriminator level
	ULD	Upper level discriminator level
	C/A SEL	Not used

**Figure 2.4: MONITOR output signals**



SCA: TTL outputs in PHA mode (TTL pulses of approx. 0.5  $\mu$ s duration. One output pulse for each input signal that falls between the ULD and LLD thresholds.

Outputs the analog TAC signals in TDC mode. The amplitude of the output signal is proportional to the time.

**REMARK:**

This output is not for spectroscopy use. It is just an indicator for the experimental setup.

Outputs the set levels in adjustment mode for control via e.g. a digital voltmeter.

### 2.2.3. Controls

Device control is performed using five buttons and two 3-position switches.

The 4 main buttons (yellow) on the front panel are used to control the device parameters. These buttons are Up/Down for each of the channels. There is also a Mode button, used to switch between Normal operation mode and different Adjust modes. To prevent accidental changes this button is hidden and accessible with a small screw driver, pencil etc. through a hole in the front panel.

Two switches define the functionality of each channel - TDC, SVA, PHA.

### 2.2.4. Indicators

Two 10-LED bars are used as Dead time / Level indicators. In normal operation mode these LED-bars indicate the dead time in %. In different adjustment modes the LED-bars give a rough indication of the currently adjusted parameter in % of the maximum value. There is no sign. The real value can be measured with a voltmeter at the front panel output.

Two additional sets of LEDs indicate the adjusted parameter (if Adj LED is lit) or currently selected range of operation in normal mode.

### 2.3. Rear panel

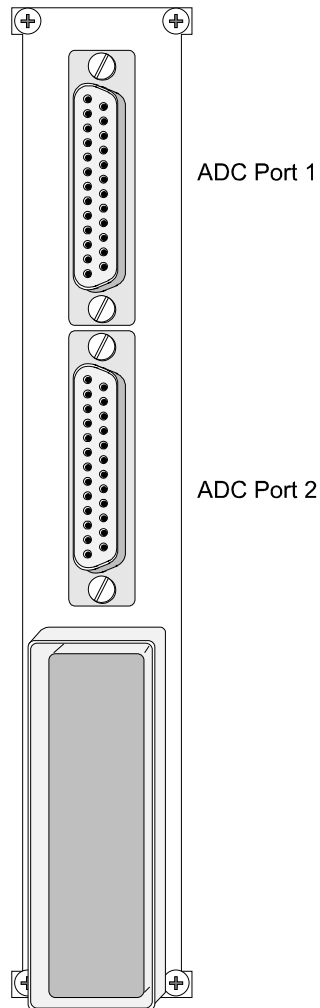
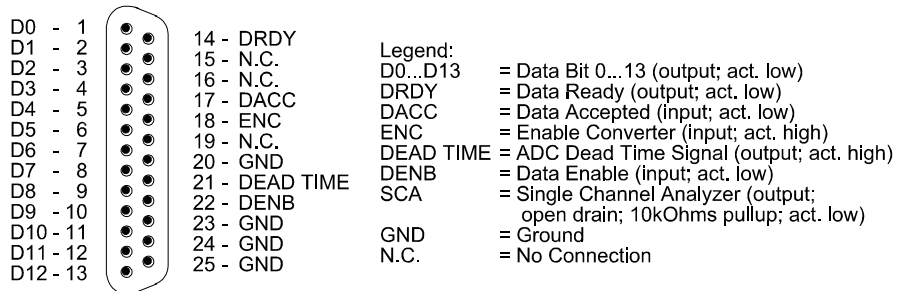


Figure 2.5: Rear panel

Data: 13 bit binary data lines and data transfer command lines, 25-pin female D-Sub connector on the rear panel.

#### 2.3.1. ADC port connectors



female 25 pin D-SUB connector

Figure 2.6: ADC port connectors

## 3. Functional Description

### 3.1. Introduction

The 7072T has three different modes of operation:

- PHA: Pulse Height Analysis
- SVA: Sampling Voltage Analysis
- TDC: Time-to-Digital Conversion

Any channel can be set in any mode of operation independently.

All settings of each channel are done via push buttons on the front panel. In normal operation the range and conversion gain are set using the corresponding UP/DOWN push buttons of each channel. To change any voltage level or the GATE mode from coincidence to anti-coincidence pressing the MODE button will switch into the adjustment mode indicated by the ADJUST LED lit. Now the corresponding voltage level is changed by the UP/DOWN buttons. Subsequent pressing the MODE button cycles through the different adjustments until you are back to normal operation.

### 3.2. Modes of operation

#### 3.2.1. Pulse Height Analysis

In this mode of operation both channels accept analog input signals between 0.025 and 10 V and measure the peak amplitudes that are higher than LLD and lower than ULD thresholds. Outside of that range between LLD and ULD there is no conversion.

To prevent triggering from noise and to adjust for small input offset voltages an ADC threshold is settable in the range of  $-100\text{ mV} \dots +1.0\text{ V}$ . The default value is  $+20\text{ mV}$ . PHA is triggered only when the input signal rises over this ADC threshold. A subsequent conversion is enabled only when the signal has been fallen under this threshold again. Thus, pile-up rejection is provided. When adjusting the ADC threshold it "pushes" the LLD if reached. Thus, the LLD level is always greater or equal to the ADC threshold.

#### 3.2.2. Sampling Voltage Analysis

In this mode of operation the corresponding channel accepts analog input signals between 0 and  $+10\text{ V}$  and measures the voltage when the GATE signal goes low to high in coincidence and high to low in anti-coincidence mode. In the SVA mode of operation, if the analog input voltage to the ADC is outside of the normal 0-10 volt range (exact range may vary slightly from unit to unit), the converted digital output will be channel zero if the voltage is greater than the normal range, and channel 8191 if it is below the normal range (firmware version V84 starting Feb 2007). The firmware version and date can be found on a label at the backside of the 7072T board.

### 3.2.3. Time-to-Digital Conversion

In this mode both channels measure the time interval between the falling edges of GATE / START and STOP signals. This time interval is converted to a digital value in the time range as been set with the yellow Up/Down buttons. The conversion range can be changed by temporarily switching into PHA or SVA mode. The START and STOP signals can be any Fast-NIM signals. If no stop signal is within the time range after a start, channel 8191 will be incremented.

### 3.3. Setting device parameters

Pressing the Mode button with a small screw driver, pencil or similar will cycle through the following adjust modes:

Adjust TDC threshold --> Adjust ADC threshold --> Adjust LLD --> Adjust ULD

--> Adjust Coincidence / Anti Coincidence --> Normal operation

An indication of being in the adjustment mode is the AGJUST LED lit.

The TDC and ADC threshold levels are set in steps of 1.22 mV while the LLD and ULD thresholds are set in steps of 4.88 mV.

The selected voltage levels can be measured on the monitor outputs.

#### 3.3.1. Adjust TDC threshold

Using the yellow Up/Down buttons the TDC threshold of the corresponding channel is set in the range of -1.0 ... -0.1 V.

#### 3.3.2. Adjust ADC threshold

Using the Up/Down buttons the ADC threshold of the corresponding channel is set in the range of -100 mV upto +1 V. If the ADC threshold reaches the LLD threshold the LLD level is "pushed" to keep it equal (not lower!) to the ADC threshold.

#### 3.3.3. Adjust LLD

Up/Down buttons set the lower level discriminator, continuously adjustable from ADC threshold to ULD threshold. If the LLD threshold reaches the ADC threshold on the way down the ADC threshold is "pushed" down to keep it equal (not higher!) to the LLD threshold.

### **3.3.4. Adjust ULD**

Up/Down buttons set the upper level discriminator, continuously adjustable from LLD threshold to +10 V.

### **3.3.5. Adjust Coincidence / Anti Coincidence**

Up/Down buttons set the coincidence/anti-coincidence GATE mode for ADC and SVA modes.

### **3.3.6. Normal operation**

When the device is in normal operation mode the UP/DOWN buttons have two different functions.

In PHA/SVA mode the Up/Down buttons select the conversion range of the ADC. The conversion range of each channel cycles through 8k - 4k - 2k - 1k - 512 - 256 - 8k - etc.

In TDC mode the UP/DOWN buttons select the time conversion range. It cycles through 50 ns - 100 ns - 200 ns - 500 ns - 1 us - 2 us - 5 us - 10 us - 20 us - 50 ns - etc.

### **3.3.7. Factory reset**

To reset all device parameters to the default values as the 7072T was shipped from the factory press both DOWN BUTTONS simultaneously during power-up.

## 4. Appendix

### 4.1. Specification

#### 4.1.1. Absolute maximum ratings

Input voltage:	any analog signal input: .....	-0.8 / +12 V
	any TTL GATE input: .....	-0.5 / +5.5 V
	any FAST-NIM input: .....	-3 / +1 V
DC input current:	any analog signal input: .....	-100 / +15 mA
	any TTL GATE input: .....	±15 mA
	any FAST-NIM input: .....	±100 mA

#### 4.1.2. Recommended operating conditions

Supply voltage:	(from NIM-BIN supply) .....	±6 V, ±12 V, ±24 V
Temperature range:	.....	0 to 50 °C

##### PHA mode:

Amplitude:	.....	0.025 ... +10 V
Pulse form:	.....	Gaussian shaped
Signal shaping time:	.....	250 ns ... 25 µs
GATE setup time:	to peak.....	>32 ns
GATE hold time:	after peak .....	>32 ns
GATE width:	.....	>65 ns

##### SVA mode:

Amplitude:	.....	0 ... +10 V
GATE width:	.....	>65 ns
GATE to sampling delay:	.....	≤32 ns

##### TDC mode:

START / STOP:	fast NIM signal .....	-16 mA, 0...-0.8 V
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#### 4.1.3. Power Requirements

Supply current:	.....	+24 V / 100 mA
	.....	+12 V / 150 mA
	.....	+6 V / 700 mA
	.....	-6 V / 430 mA
	.....	-12 V / 200 mA
	.....	-24 V / 90 mA

**4.1.4. Connectors**

**SIGNAL Input**

Input impedance: dc coupled ..... 1 k $\Omega$   
 Connector type: ..... BNC

**GATE / START Input**

PHA/SVA mode:  
 Input impedance: COINCidence mode ..... 4.7 k $\Omega$  to +5 V  
 ANTIcoincidence mode ..... 4.7 k $\Omega$  to GND  
 Input HIGH voltage: ..... min. +2.5 V  
 Input LOW voltage: ..... max. +0.4 V  
 Pulse width: ..... > 100 ns  
 TDC mode:  
 Input impedance: diode protected ..... 50  $\Omega$   
 Threshold voltage: ..... -1 V ... -100 mV, in steps of 1.22 mV  
 Pulse width: below threshold ..... >2 ns  
 Sensitivity: ..... falling edge initiates time conversion

**STOP Input**

Input impedance: diode protected ..... 50  $\Omega$   
 Threshold voltage: ..... -1 V ... -100 mV, in steps of 1.22 mV  
 Pulse width: below threshold ..... >2 ns  
 Sensitivity: ..... falling edge terminates time conversion

**MONITOR Output**

Output impedance: ..... 1.4  $\Omega$  typ.  
 Output current: .....  $\geq$  26 mA, 34 mA typ.  
 Short-circuit current:  $V_{OUT} = 0 V$  .....  $\geq$  40 mA, 54 mA typ.  
 Gain Error: .....  $\leq \pm 2\%$  typ.  
 Offset: .....  $\leq \pm 4$  mV typ.

**4.1.5. Default Settings**

ADC Conversion range: ..... 8192  
 TDC Time range: ..... 50 ns  
 TDC threshold: ..... -500 mV  
 ADC threshold: ..... +20 mV

LLD: ..... +25 mV  
 ULD: ..... +9.95 V  
 Coinc/Anti-coincidence: ..... Coincidence

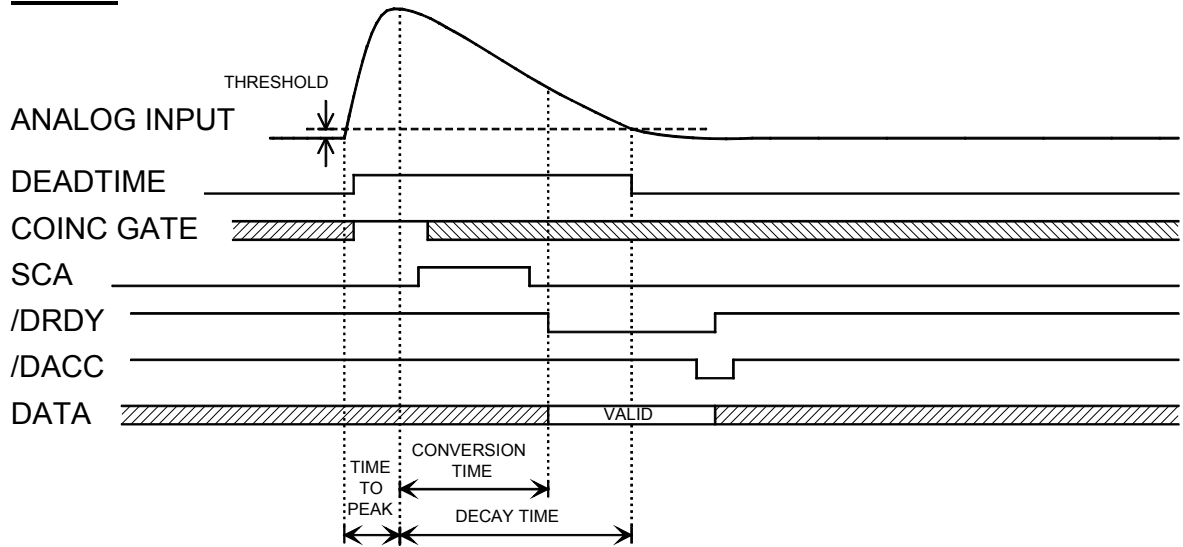
**4.1.6. Level adjustment ranges**

TDC threshold: ..... -1.0 V ... -100 mV, in 1.22 mV steps  
 ADC threshold: ..... -100 mV ... +1.0 V, in 1.22 mV steps  
 LLD: (ADC th < LLD ≤ ULD) ..... +20 mV ... +10 V, in 4.88 mV steps  
 ULD: (ULD ≥ LLD) ..... +20 mV ... +10 V, in 4.88 mV steps

**4.1.7. ADC Signal Timing**

**General ADC Signal Timing**

**7072:**



DEADTIME = Time-to-peak + MAX(DecayTime; ConversionTime)

**Figure 4.1: General ADC Signal Timing**



## 4.2. Performance characteristics

### 4.2.1. ADC

Range:	..... 256, 512, 1024, 2048, 4096, 8192
Conversion time:	fixed conversion time ..... 500 ns
Countrate capability:	..... > 1.000.000 events/s
ADC deadtime:	time-to-peak + 500 ns fixed conversion time + data transfer time of 100 ns to buffer (there could be an additional dead time if the MCA can not accept the data rates generated by the 7072T - this depends on the MCA used) ..... Typical ADC deadtime for fast rising input pulses is less than 2 us per event using FAST ComTec MCAs
Resolution:	8k range, 500ns flat top pulses ..... $\leq 3.4 \text{ chs}^1$ FWHM
Integral non-linearity:	linear fit ..... typ. $\pm 0.16\%$ @ 8k range linear fit ..... typ. $\pm 0.16\%$ @ 4k range
Differential non-linearity:	including effects from integral non-linearity ..... $\pm 1.1\%$ @ 8k range for 99% of usable channels ..... $\pm 0.7\%$ @ 8k range including effects from integral non-linearity ..... $\pm 0.7\%$ @ 4k range for 99% of usable channels ..... $\pm 0.5\%$ @ 4k range
Peak shift:	upto 700 kcps, SVA mode ..... $\pm 0.006\%$ upto 1000 kcps, SVA mode ..... $\pm 0.08\%$
Unused channels:	..... approx. top 1% of range
Analog bandwidth:	..... 3.3 MHz
GATE to sampling delay:	SVA mode: ..... 0 ... 32 ns

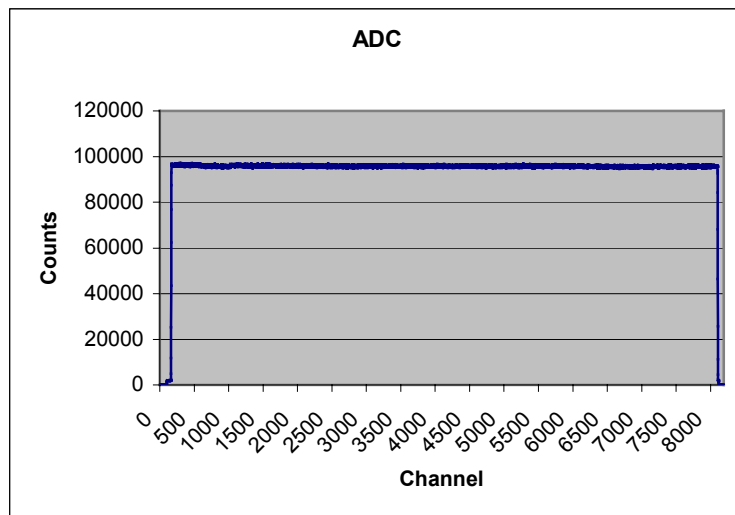


Figure 4.2: PHA, typical noise spectrum

<sup>1</sup> channels

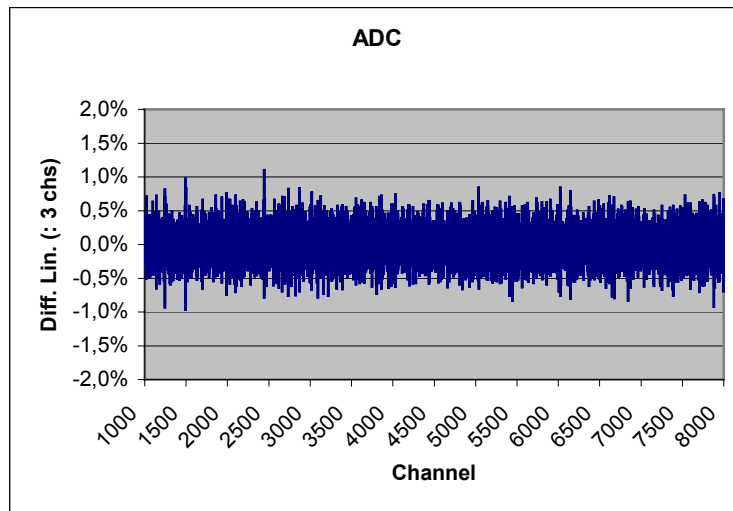


Figure 4.3: ADC, typical differential linearity plot

#### 4.2.2. TDC

Time range:	..... 50 ns, 100 ns, 200 ns, ..... 500 ns, 1 $\mu$ s, 2 $\mu$ s, ..... 5 $\mu$ s, 10 $\mu$ s, 20 $\mu$ s
Usable times:	(start delay) ..... approx. > 6...8 ns
Conversion range:	..... 256, 512, 1024, 2048, 4096, 8192
Resolution:	50 ns range ..... typ. $\leq$ 4.1 chs FWHM
Integral non-linearity:	50 ns range, linear fit ..... typ. $\pm$ 0.12%
Differential non-linearity:	50 ns range ..... typ. $\pm$ 0.5% for 99% of usable channels ..... $\pm$ 0.4%
Count rate stability:	upto 100 kcps ..... $\pm$ 0.003%

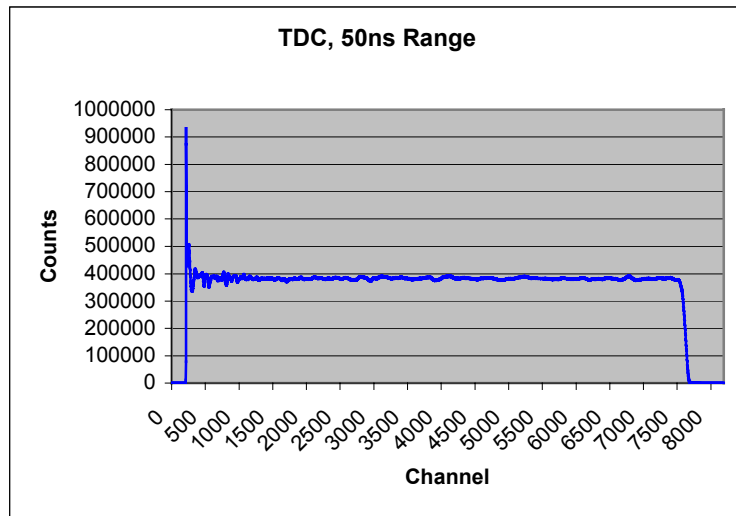


Figure 4.4: TDC, typical noise spectrum (50ns range)

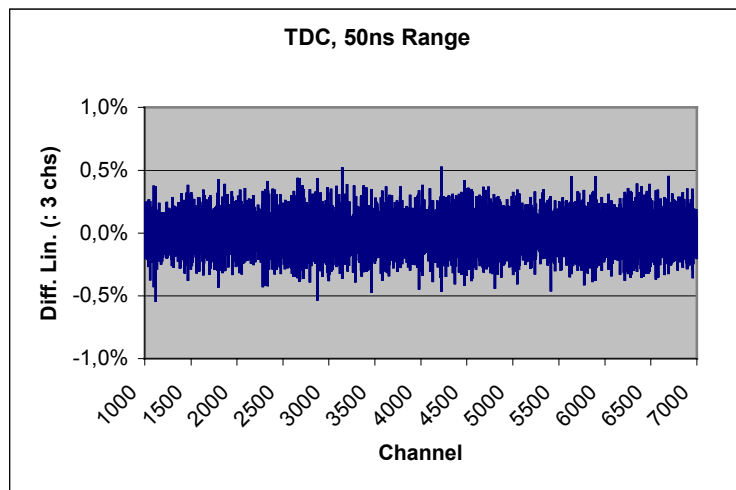


Figure 4.5: TDC, typical differential linearity plot (50ns range)

### 4.3. Physical

Physical size: single width NIM module (1.35 x 8.71 inches; 3.43 x 22.13 cm)  
as per TID - 20893 (rev.)

Shipping weight: ..... 1.8 kg (net 1.0 kg)