Model 7029A
Constant Fraction Differential Discriminator

Operating Manual

STANDARD WARRANTY

for

FAST ComTec Products

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Before being approved for shipment, each FAST ComTec instrument must pass a stringent set of quality control tests designed to expose any flaws in materials or workmanship. Permanent records of these tests are maintained for use in warranty repair and as a source of statistical information for design improvements.

Repair Service

If it becomes necessary to return this instrument for repair, it is essential that Customer Services be contacted in advance of its return so that a Return Authorization Number can be assigned to the unit. Also, FAST ComTec must be informed, either in writing, by telephone +49-89-665180-50 or by facsimile transmission +49-89-66518040, of the nature of the fault of the instrument being returned and of the model, serial, and revision ("Rev" No. on rear panel - if applicable) numbers. Failure to do so may cause unnecessary delays in getting the unit repaired. The FAST ComTec standard procedure requires that instruments returned for repair pass the same quality control tests that are used for new-production instruments. Instruments that are returned should be packed so that they will withstand normal transit handling and must be shipped **PREPAID** via Air Parcel Post, Air Freight or United Parcel Service to the FAST ComTec repair center in Oberhaching, Germany. The address label and the package should include the Return Authorization Number assigned. Instruments being returned that are damaged in transit due to inadequate packing will be repaired at the sender's expense, and it will be the sender's responsibility to make claim with the shipper. Instruments not in warranty will be repaired at the standard charge unless they have been grossly misused or mishandled, in which case the user will be notified prior to the repair being done. A quotation will be sent with the notification.

Damage in Transit

Shipments should be examined immediately upon receipt for evidence of external or concealed damage. The carrier making delivery should be notified immediately of any such damage, since the carrier is normally liable for damage in shipment. Packing materials, waybills, and other such documentation should be preserved in order to establish claims. After such notification to the carrier, please notify FAST ComTec of the circumstances so that assistance can be provided in making damage claims and in providing replacement equipment, if necessary.

CONTENTS

SAFETY INSTRUCTIONS AND SYMBOLS

This manual contains up to three levels of safety instructions that must be observed in order to avoid personal injury and/or damage to equipment or other property. These are:

DANGER Indicates a hazard that could result in death or serious bodily harm if the safety instruction is not observed.

WARNING Indicates a hazard that could result in bodily harm if the safety instruction is not observed.

CAUTION Indicates a hazard that could result in property damage if the safety instruction is not observed.

Please read all safety instructions carefully and make sure you understand them fully before attempting to use this product.

SAFETY WARNINGS AND CLEANING INSTRUCTIONS

DANGER Opening the cover of this instrument is likely to expose dangerous voltages. Disconnect the instrument from all voltage sources while it is being opened.

WARNING Using this instrument in a manner not specified by the manufacturer may impair the protection provided by the instrument.

Cleaning Instructions

To clean the instrument exterior:

- Unplug the 683 from the ac power supply.
- Remove loose dust on the outside of the instrument with a lint-free cloth.
- Remove remaining dirt with a lint-free cloth dampened in a general-purpose detergent and water solution.
  Do not use abrasive cleaners.

CAUTION To prevent moisture inside of the instrument during external cleaning, use only enough liquid to dampen the cloth or applicator.

- Allow the instrument to dry completely before reconnecting it to the power source.

FAST COMTEC MODEL 7029A
CONSTANT FRACTION DIFFERENTIAL DISCRIMINATOR

1. DESCRIPTION

1. INTRODUCTION

1.1 General Description

The model 7029A is a fully dc-coupled differential constant fraction discriminator with a dynamic range of up to 700:1 for the base line discriminator (BLD) part and up to 300:1 for the single channel analyzer (SCA) part. This unit provides optimum time resolution for many detector types and applications, for example:

CF – constant fraction mode for fast detectors,
SR – slow risetime reject mode for germanium detectors.

Additional features which are only provided by the Model 7029A are outlined in section 6.

The model 7029A accepts negative polarity pulses at its 50Ω-terminated, dc-coupled input. For positive polarity input pulses see section 6. The constant fraction composite signal is formed by the algebraic sum of a direct (by a fraction f) signal path and a delayed, unattenuated path. The delay time is selectable according to the propagation delay of a 50Ω cable. Careful selection of fraction and delay provides full compensation of timing distortions due to both amplitude and risetime variations in the input signal. An output signal (BLD outputs) is generated whenever the input signal exceeds the selected threshold (front panel 10-turn dial potentiometer). This part is functionally identical with the normal constant fraction discriminators.

The Model 7029A provides, in addition, fast signal level discrimination. Full range (- 10 mV to – 2.5 V) lower level (LLD) and upper level (ULD) controls allow selection of signal amplitudes. A time signal (SCA outputs with the same time stability as the BLD outputs) is only enabled for signal amplitudes within the selected window. With the standard version four simultaneous, independent output signals (BLD and SCA) are provided. The negative NIM current outputs are derived as fixed-width pulses. The width of the positive NIM voltage outputs is adjustable in normal dead time mode. The width then refers to the internal deadtime setting as required to suppress spurious outputs due to input anomalies.

For additional outputs or change of the width of the negative output signals see section 6.

The ULD positive voltage output indicates (with ULD mode on) the upper level setting was exceeded.
The wide dynamic range of the Model 7029A permits its use in many timing applications without the need for fast pulse amplifiers. The present model provides the simultaneous use as a normal (BLD outputs) and as a differential (SCA outputs) constant fraction discriminator. Additional features and options (on customer specification) are outlined in section 6.

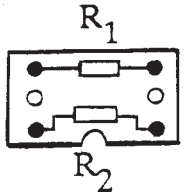
1.2 Setup information

1.2.1 Selection of modes

Mode switch	Comments
CF	constant fraction discriminator
SR	constant fraction discriminator with slow risetime reject
ULD on	differential constant fraction discriminator – window mode (SCA)
ULD off	integral constant fraction discriminator only LLD in operation
DT n	normal deadtime operation, deadtime given by the width of the positive output signals
DT up	update deadtime operation

1.2.2 Fraction

The factory set fraction f = 0.4. If a different fraction is required, the plug-in module (on the printed board) has to be changed as follows:



$R_0 = 50\Omega$

$R_1 = R_0 \times f$

$R_2 = R_0 / f$

2. SPECIFICATONS

2.1 Inputs

Input	from – 5 mV to about – 3.5 V linear pulses in the BLD part (ref. to common mode range of ultra fast comparators) and – 10 mV to – 2.5 V linear pulses in the SCA part, risetime > 700ps, typically R_{in} = 50Ω, dc-coupled front panel BNC connector minimum input pulse width > 1 ns (BLD part)
Delay	two BNC connectors for an external delay cable to form the internal constant fraction signal. For specific length see section 4.2.3.

2.2 Outputs

Inspect	displays output signal of zero crossing discriminator for use in trimming the time walk
BLD neg.	negative current output, providing – 32 mA into 50Ω, risetime ≈ 2 ns, pulse width < 5 ns nominal, dc-coupled
BLD pos.	positive voltage output providing 1.5 V (min.) into 50Ω, risetime ≈ 4 ns, width (in normal deadtime mode) adjustable by front panel trimming potentiometer, the width then determines the internal deadtime
SCA neg.	negative current output, providing – 32 mA into 50Ω, risetime ≈ 2 ns, pulse width < 5 ns nominal, dc-coupled
SCA pos.	positive voltage output, providing 2 V (min.) into 50Ω, risetime ≈ 4 ns, width as BLD pos.
ULD	positive voltage output, providing 1.5 V (min.) into 50Ω, risetime ≈ 4 ns, width as BLD pos.

2.3 Controls

Threshold Front panel 10-turn locking dial potentiometer to set acceptance level for input pulses (range ≈ - 5 mV to – 1.2 V)

LLD Front panel 10-turn locking dial potentiometer to set lower discriminator threshold for input pulses in the SCA part (range ≈ - 10 mV to – 2.5 V)

ULD Front panel 10-turn locking dial potentiometer to set upper discriminator threshold for input pulses in the SCA part (mode ULD on; range ≈ - 10 mV to – 2.5 V)

Z/C adjust (walk adjust) front panel trimming (screwdriver) potentiometer to compensate walk of the internal zero crossing discriminator

CF-SR front panel two position switch to select the modes of timing

ULD on/off selects window or integral mode in the SCA part

DT n/up selects mode of deadtime operation; in n = normal position the deadtime is given by the width of the positive output signals (BLD, SCA or ULD); width is adjustable by a front panel (screwdriver) trimming potentiometer, in update mode any input signal arriving during the blocking period of the previous pulse, causes the deadtime to be extended by an amount equivalent to the blocking width

2.4 Indicators

Rate LED indicates activity of the discriminator. Colour of the LED changes by count rate of the BLD part: green up to ≈ 5 kHz, orange from ≈ 5 kHz to ≈ 10 kHz, red. above (for statistical input pulses)

2.5 Performance

Dynamic range 700:1 for the BLD part (regarding the linearity of the input signals) and 300:1 for the SCA part as specified above

Walk in CF mode for a 1 ns risetime pulse over a 100:1 range (reference – 2.5 V) ≈ 60 ps, typically ± 40 ps

Count rate more than 50 MHz, limited by deadtime setting

Pulse pair resolution
less than 10 ns, or as limited by deadtime

Threshold stability
better than ± 0.02% /°C (± 200 ppm/ °C)

Linearity ± 0.25% integral

Temperature range 0
°C to 50 °C

2.6 Delay Cable

typ. lengths for fast pulses ≈ 0.5 m to 1 m for pulses; from slow detectors, (e.g. germanium) 1.5 m to 4 m for better determination of the cable length see also section 4.2.3; for very fast risetimes the internal cable lengths have to be taken into account, see section 4.2.3

2.7 Power Requirements

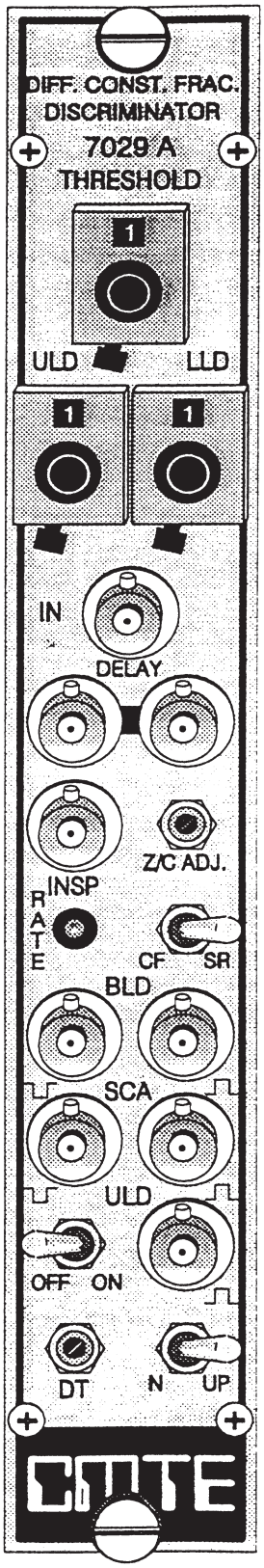
+ 6 V, 150 mA, - 6 V, 450 mA (standard version)

2.8 Physical

Size single width NIM module (1.35 x 8.71 inches; 3.43 x 22.13 cm) per TID – 20893 (rev.)

3. CONTROLS, CONNECTORS AND INDICATORS

3.1 Front Panel



Threshold setting from –5mV to –1.2V for signal acceptance

Upper level discriminator (SCA part) setting from –10mV to –2.5V linear

Lower level discriminator (SCA part) setting from –10mV to –2.5V linear

Input accepts –5mV to –3.5V (BLD mode) linear signals, min. input width ≈700ps

Connectors for external delay cable

Walk inspect allows observation for zero crossing discriminator adjustment

Z/C adjust for the zero crossing mark in CF and SR mode

Rate LED indicates count rate

mode switch selects CF or SR operation

negative output supplies –32mA into a 50Ω load

positive output (BLD part) supplies a TTL logic signal into a 50Ω load

negative output supplies –32mA into a 50Ω load

positive output (SCA part) supplies a TTL logic signal into a 50Ω load

mode switch ULD on/off

positive output supplies a TTL signal into a 50Ω load if the ULD mode is on and the input signal has exceeded the ULD setting

Width control set the width of all positive outputs and the internal deadtime (in n – DT mode)

selects normal deadtime (n) or up date deadtime (up)

3.2 Rear Panel

Several options (on customer specification) are available with the appropriate connectors at the rear panel. For options see section 6.

4. OPERATION

4.1 General

The purpose of this section is to familiarize the user with the operation of the model 7029A and to confirm that the unit is working properly. The module can be operated in many different system configurations, therefore it is difficult to give explicit operating instructions. However, if the guide line of the listed procedures is followed, the experimentalist will gain sufficient experience with this unit to use it properly.

4.1.1 Bock Diagram

The blockdiagram of the model 7029A, as given in fig. 2, is only intended to clarify the different signal paths within the unit.

4.2 Laboratory Bench Tests

Basic performance tests of the model 7029A may be exercised either in a rack mounted BIN or on a laboratory bench with the unit powered by an extender cable from a NIM BIN (TID-20893). It is recommended that electrical connections be made with BIN power off. On installation or after BIN power failures it is recommended to toggle the deadtime switch, in order to reset the internal logic.

4.2.1 Input

Suitable driving pulses may be obtained from laboratory pulsers or pulse generators, or readily available detector pulse signals. The input network is protected for pulses exceeding 5V in amplitude. But the user should keep in mind that the linearity is limited by the common mode range of the ultra fast comparators in the input stages.

4.2.2 Operating Mode

The selection of the operating mode depends on the requirements of the experiment. In the CF mode the timing is derived from a comparison between an attenuated pulse (f = 0.4, factory set) and a delayed pulse (delay time t_d). The derived time mark is theoretically independent of the pulse height. For a detailed description of the principle see e.g.: *D.A. Gedcke and W.J. McDonald, Nucl. Instr. & Meth. 56 (1968) 253, M.R. Maier and P. Sperr, Nucl. Instr. & Meth. 87 (1970) 13.*

The choice of the fraction f and the time delay t_d (see also section 4.2.3) depends on the detector and the experimental setup.

In the SR mode – constant fraction with slow risetime reject – a further option to handle the longer risetimes of e.g. solid state detectors is provided. Normally the timing mark for the CF is derived with the presumption that the threshold level (or here also called baseline discriminator BLD) has been set quite low and this level is exceeded prior to the derivation of the time mark. In the case of long varying wavefronts of the input pulses (and if relatively short delay cables are used) the timing condition as given above may not be valid. In that case the level discriminator may switch late. The resulting timing mark will represent some mixture of the intended CF timing with leading edge timing. This effect causes tailing or even a satellite peak in a time spectrum. In the SR mode an option is included which rejects pulses which have not exceeded the threshold level prior to the derived CF timing mark. Some loss of count rate efficiency in the SR mode is obvious.

4.2.3 Delay

Normally the delay cable used should provide a delay less than the risetime t_r of the input pulses. Theoretically the total delay required can be calculated from the following relation:

$$t_d \approx (1\text{-}f) \times t_r$$

which was found to be the optimum for most applications (f = fraction, t_r = risetime of the input signal, t_d = total delay).

The internal delay (cable lengths BNC connectors to printed board) is about 0.5 ns. This must be corrected in picking a suitable cable ($t_d = t_{cable} + 0.5$ ns).

For very fast pulses t_r < 2 ns) it is recommended to measure the delay direct at the input of the high speed comparator (pin 7 and pin 8 of C2) and if necessary to directly install a delay cable omitting the front panel BNC connectors.

4.2.4 Z/C Adjust – Walk Trim

The adjustment of the amplitude sensitive variation of the timing mark has to be carried out carefully. Proper adjustment is only possible when the dc-offset present at the input is small. Thus detector leakage or dark current errors must be minimized before attempting adjustment.
Laboratory trimming of the unit using a fast pulse generator for the first test measurement is recommended. Different settings of the Z/C adjust (or walk adjust) potentiometer should be tried in order to find the optimum time resolution.
When the model 7029A is used with the intended detector, time resolution has to be trimmed experimentally by successive measurements in the setup at hand, because the resolution depends on many parameters such as fraction, threshold (BLD), delay and Z/C adjustment. A quantitative control is available by monitoring the front panel inspect output with an oscilloscope, externally triggered with the fast BLD output.
For fast detectors the inspect output (not to be terminated with 50Ω) should appear between – 0.2 V and – 0.4 V and should look as shown in fig. 1. For slower detectors, a noise band between the levels may be seen, with transitions to high and low of about equal intensity. Symmetrical center setting should be avoided as the new ultra fast comparators deviate from their optimum performance in this setting.

4.2.5 Outputs

The output logic pulses from the model 7029A are intended to drive 50Ω loads through any reasonable length of suitable 50Ω coaxial cable (such as RG-58).
As the setting of the widths of the positive output signals is consistent (in DT –n) with the internal dead time, the user should set this control due to the requirements of the pulse rate for the given experiment. For the option of additional outputs see section 6.

5. CIRCUIT DESCRIPTION

5.1 General

The model 7029A provides the advantages that various modes of operation (CF/SR, ULD on/off, DT n/up) can be chosen by selecting front panel switches. The plug in fraction module can be easily changed. A great advantage as compared to other differential constant fraction discriminators is due to the BLD outputs.
Therefore the model 7029A can be simultaneously used as a „normal" constant fraction and as a differential constant fraction discriminator. Possible applications are given in section 6. The bulk of the logic signal processing is executed in emitter-coupled fast integrated circuit logic (ECL – 10 KH series). Reference diodes are used to stabilize all threshold voltages.

5.2 CF- and SR-Mode

The input signal is split in a network to serve the four identical ultra fast comparators C1 to C4 (see fig. 2). The comparator C1 provides an ECL logic pulse (-1.7V to –0.4V) whenever the lower baseline threshold is exceeded. The output signals (inverting and non-inverting) are applied to gates G1 and G2. The delayed input pulse is applied to the non-inverting input of C2; the prompt but attenuated signal (determined by the fraction setting) is applied to the inverting input of C2. The difference signal of these inputs is a bipolar pulse whose zero crossing defines the time mark. The time walk of the bipolar signal is theoretically zero. Finite errors, such as small dc-shifts at the input, offset biases of the comparators, as well as their finite gain-band widths cause some time shifts (or walk). With the front panel Z/C adjust - by monitoring the inspect signal (one output of C2) – these errors can be minimized. The output of C2 is applied to gate G1. In normal operation the first pulse to G1 is provided from comparator C1 and the signal from C2 (with the exact time mark) is then processed through gate G1. The output of this gate is fed to the clock enable input of a master-slave type D flip-flop (FF1). The Q-output of FF1 is fed to a bus driver (D1) which converts the ECL levels to fast NIM levels forming the fast BLD output signal. The Q-output of FF1 is also used as clock for FF2 and FF3 and as Set fro FF4, respectively. The deadtime stage, set between FF1 and FF4, is formed (normal or up date mode) using four line receivers (see fig. 3).
In the SR mode pulses which do not satisfy the BLD setting prior to the derived constant fraction mark are locked out and rejected. In this mode the CF/SR switch is left open. The inverting output of C1 is processed through gate G2. The output signal of G2 is applied to the data input of FF1, therefore timing marks derived with a BLD (comparator C1) switching late are blocked.

One output (Q) of FF4 is fed to an ECL-to-TTL translator T1 to form the positive BLD output signal and to the driver stage of the LED´s which indicate the count rate of the constant fraction discriminator. The Q-output of FF4 is used as clock for FF2 and FF3 (for details see fig. 3).
The lower level discriminator (LLD) and upper level discriminator (ULD) thresholds can be set at the comparators C3 and C4. The generated output signals are processed through gates G3 and G4 and fed to the Data inputs of the master-slave type D flip-flops FF2 and FF3, respectively. Note that the relevant clock pulse is always provided by FF1. In the ULD „on" mode (switch left open) signals from imputs which exceed the ULD are processed through G3 and FF3 and are converted by T3 to a positive output pulse (ULD out), but block the gates G5 and G6. Only input signals within the LLD and ULD level settings are processed through gates G5 and G6 and are converted in D2 to a negative fast NIM and in T2 to a positive TTL output (SCA outputs). In the ULD "off" mode, all input signals which exceed the LLD threshold setting, generate a signal at the SCA outputs.

6. SPECIAL FEATURES AND OPTIONS

In this section some special features of the model 7029A and additional options, which are available on request are listed.

Power Supply

Normally ± 6V from a standard NIM BIN
or, on customer request, ± 12 V from a NIM BIN, at extra charge

Input Polarity

The standard version of the 7029A requires negative input polarity. In some cases the output pulses of detectors have positive polarity. In this case a signal transformers (e.g. Ortec IT 100) is required.

Additional outputs

on customer specification a second fast BLD and/or a second fast SCA output is available at the rear panel, at extra charge.

Output Width

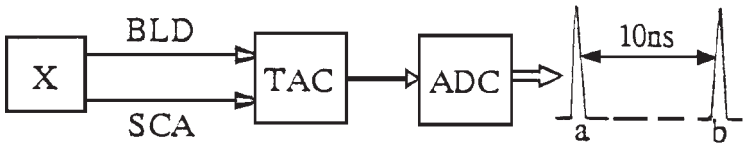
The output width is factory set to about 5 ns.
on customer request the width of the negative output can be made larger within meaningful values regarding internal settings, extra charge applies.

Thresholds

In the standard version the threshold setting for BLD, LLD and ULD is performed via front panel potentiometers. If necessary the threshold voltages can also be supplied externally (e.g. computer-controlled) via rear panel connectors.

"Quick" Time Calibration

The second negative outputs (BLD and/or SCA) on the rear panel can be (factory set) delayed by a fixed time (e.g. ≈ 10 ns equivalent to about 2 m of cable) with respect to the front panel outputs. The user can once exact calibrate this delay and has then the possibility to use this further on as a quick reference calibration for time circuits.

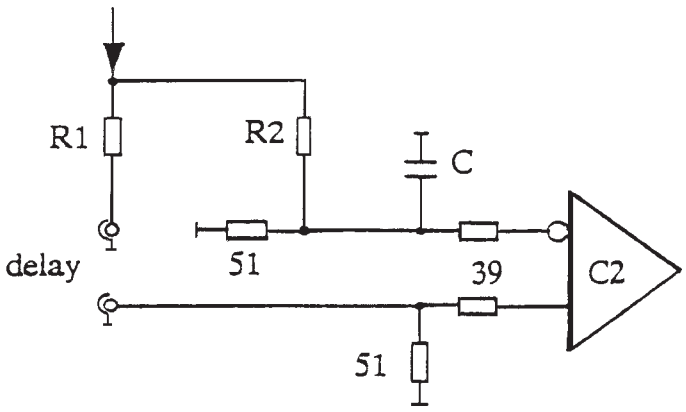


a: SCA output (TAC-stop) from front panel
b: SCA output (TAC-stop) from rear panel

"Signal Shaping"

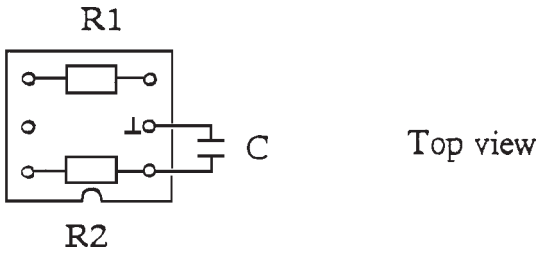
For some detector systems considerable improvements in time resolution (using the BLD outputs) can be achieved using small fractions f ≈ 0.1 and „RC-shaping" of the attenuated signal (examples are given in the literature). The circuit diagram for this option is sketched in the following figure. The capacitor C can be easily implemented on the fraction module as shown below

With $R_1 = R_0 \times f$ and $R_2 = R_0 / f$



$C \approx 10pF$ to $\approx 22pF$

$t_d \approx R_0 \times C + (1-f) \times t_r$ $\qquad R_0 = 50\Omega$

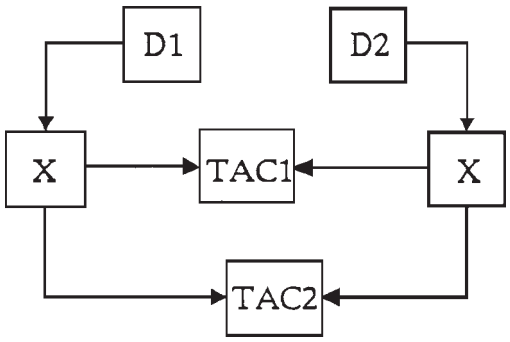


The best values for the fraction f, the capacitor C and the delay t_d have to be determined experimentally.

Note: If a different fraction bridge is inserted (disregarding the node of the socket) be sure that R1 is always the upper resistor

Use as normal and as differential constant fractions discriminator
(conventional two detector start-stop configuration)

X: model 7029A
TAC1: complete time spectrum – start-stop with BLD outputs
TAC2: selected time spectrum – start-stop with SCA outputs



In the configuration given above it is also possible to use only one TAC. The SCA outputs must then be used in coincidence with a routing system.

In the standard coincidence set-up (TAC start-stop with the BLD outputs), the SCA outputs can be used via coincidence as gate signal for an ADC. This might be convenient if an external control of the LLD and ULD threshold settings is used.

7. Diagrams

7.1 Inspect Signals

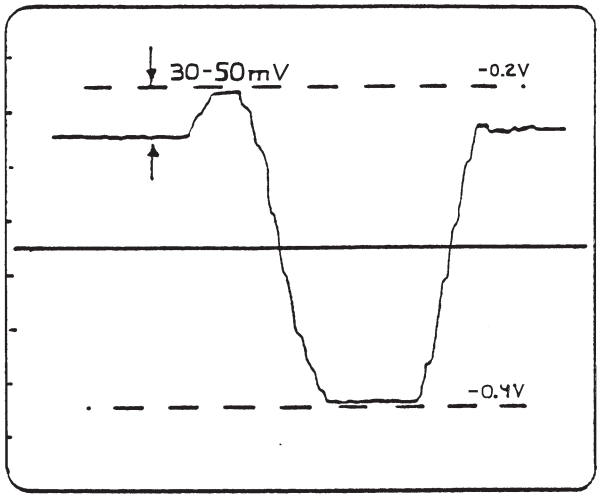
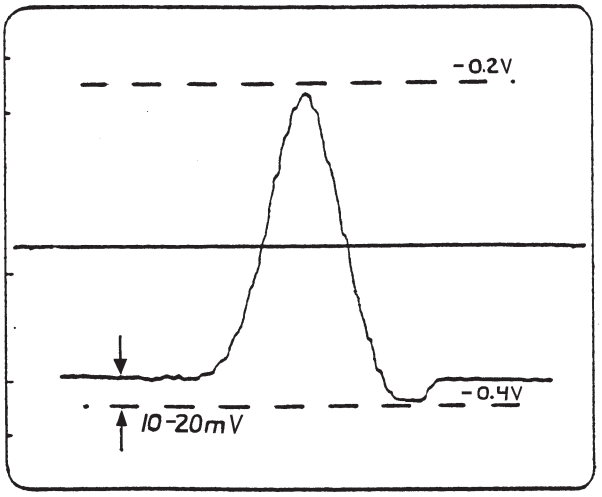
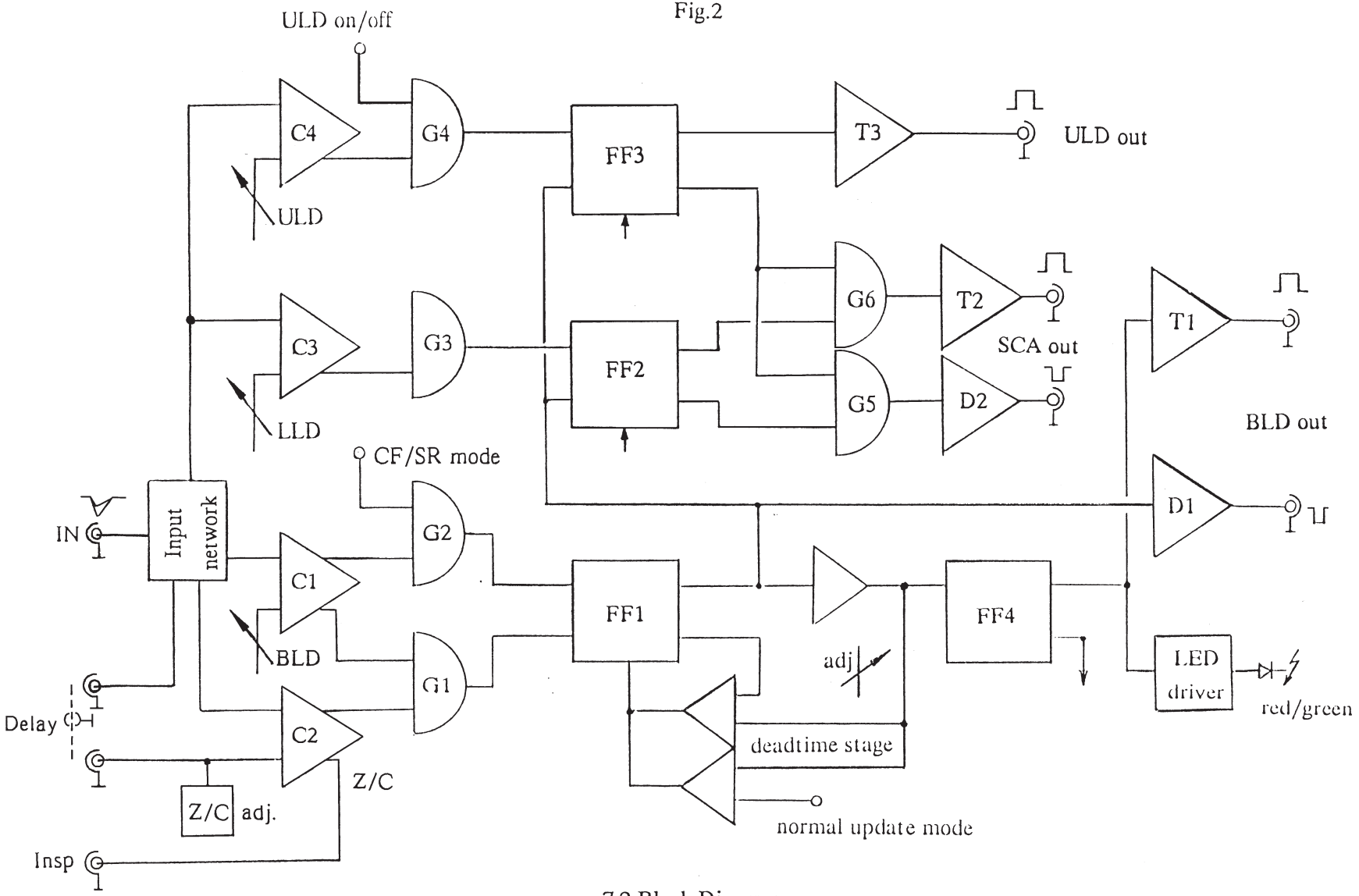


Fig.1



Avoid symmetrical setting

Fig.2



7.2 Block Diagram

8. FACTORY SERVICE

This instrument can be returned to the FAST ComTec factory for service and repair at a nominal cost. Our standard procedure for repair ensures that the same quality control and checkout procedures used for a new FAST ComTec instrument will be used for your repaired unit. Before sending instruments for repair, you must contact our Customer Service Department, +49-89-665180-50, to obtain a Return Authorization Number and shipping instructions. Be sure to write the Return Authorization Number on the address label and on the package.

BIN/MODULE CONNECTOR PIN ASSIGNMENTS FOR AEC STANDARD NUCLEAR INSTRUMENT PER DOE/ER 0457T

Pin	Function	Pin	Function
1	+3 V	23	Reserved
2	-3 V	24	Reserved
3	Spare Bus	25	Reserved
4	Reserved Bus	26	Spare
5	Coaxial	27	Spare
6	Coaxial	28	+24 V
7	Coaxial	29	-24 V
8	200 V dc	30	Spare Bus
9	Spare	31	Spare
10	+6 V	32	Spare
11	-6 V	33	117 V ac (Hot)
12	Reserved Bus	34	Power Return Ground
13	Spare	35	Reset (Scaler)
14	Spare	36	Gate
15	Reserved	37	Reset (Auxiliary)
16	+12 V	38	Coaxial
17	-12 V	39	Coaxial
18	Spare Bus	40	Coaxial
19	Reserved Bus	41	117 V ac (Neutral)
20	Spare	42	High-Quality Ground
21	Spare	G	Ground Guide Pin
22	Reserved		