2128

Constant-Fraction-Discriminator

Operating Manual

Grünwalder Weg 28, D 8024 Oberhaching
Germany

Model 2128
Constant Fraction Discriminator

Features:

- **100 MHz Count Rate**
- **1000: 1 Dynamic Range**
- **Five Operating Modes**
- **Walk < 30 ps typically for 100: 1 Range**
- **Simultaneous Dual Positive and Negative Outputs**
- **Multicolor Count Rate Indicator**
- **DC coupling**

Description:

The Model 2128 is a fully dc-coupled constant fraction discriminator with a dynamic range of up to 1000: 1. Three operating modes provide optimum time resolution for many detector types and applications. For example:
CFT-Constant fraction mode for fast detectors
CFRR-Slow rise time reject mode for Ge detectors
LET-Leading edge mode for single photon counting

In addition, internallyselectable program modules provide for
1) User change of fraction from the standard 40%,
2) Operation of the unit as a Zero Crossing Discriminator for bipolar inputs, and
3) Operation of the unit as a Leading Edge Discriminator without termination of the delay ports.

The Model 2128 has a dc-coupled 50 ohm input which accepts negative pulses. The constant fraction composite signal is formed by the algebraic sum of a direct, attenuated signal path and a delayed. unattenuated path. The delay time is user selected by cable delay. Optimum selection of this external delay provides full compensation for timing distortions due to both amplitude- and rise time variations in the input signal.
Four simultaneous, independent output signals are provided. The two positive outputs are adjustable in width, the width duration sets the internal dead time required to suppress spurious outputs due to input signal anomalies. The two negative outputs are fixed-width pulses keyed to the start of the dead time period.
The front panel WALK ADJUST control and INSPECT OUTPUT permit the user to trim the time walk characteristics of the experimental setup for optimum timing resolution. A novel frontpanel LED indicates count rate by color change.

Specifications:

INPUTS
INPUT - Accepts - 5 mV to - 5 V linear pulses: width:≥ 1ns, Zin= 50 Ohms, dc coupled; front panel BNC connector.
DELAY - 2 front panel BNC connectors accept 50 Ohm delay cable to form the internal constant fraction signal.

OUTPUTS
WALK INSPECT - Displays signal of zero crossing discriminator for use in trimming time walk.

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FAST ComTec GmbH
Grünwalder Weg 28A • 82041 Oberhaching • Germany
phone: 49-(0)89 665180 0 • fax: 49-(0)89 665180 40 • http://www.fastcomtec.com

LEADING EDGE - (With fraction module inserted) displays leading edge discriminator output.
OUTPUTS Two independent negative current outputs, each providing -32 mA into 50 ohms; rise time < 3 ns, pulse width 5 ns nominal, dc coupled.
OUTPUTS - (+)- Two independent positive voltage outputs providing 2 V (minimum) into 50 ohms, rise time< 10 ns, width adjustable by adjacent width trimming potentiometer, which also determines internal dead time.
CLIP CABLE (rear panel) - 2 BNC connectors accept 50 Ohm delay cable to adjust width of the negative output pulses: controlled by adjacent IN-EXT switch.

CONTROLS
THRESHOLD - Front panel 10-turn locking dial potentiometer to set acceptance threshold for input pulses: range - 5 mV to - 1V.
INSPECT WALK - Front panel trimpot to compensate walk of the internal zero crossing discriminator.
LEADING EDGE WIDTH - Frontpanel trimpot: With fractionmodule inserted sets leading edge width to input pulse duration: With zerocross module inserted sets leading edge width beyond Z/C point of the input signal.
CFRR-CFT-LET - Front panel three position rotary switch to select constant fraction with slow rise time reject (CFRR), basic constant fraction timing (CFT), or leading edge timing (LET) modes of operation.
OUTPUT WIDTH - Front panel 22-turn screwdriver adjustable potentiometer to set width of slow positive output pulse, which is equal to the internal dead time of the discriminator - max. setting: 1.5 micro sec.
IN—EXT (rear panel) - Toggle switch allows use of external cable to widen negative outputs.

PERFORMANCE
DYNAMIC RANGE - 1000 : 1
CF MODE WALK ≤±50ps (typically ±30ps) for-3OmV to -3V range with <2 nsec rise time.
COUNTING RATE - to 100 MHz, limited by dead time (OUTPUT WIDTH setting).
PULSE PAIR RESOLUTION - <10 ns, or as limited by dead time.
THRESHOLD STABILITY - Better than ±0.02 %/°C (± 200 ppm/°C)
TEMPERATURE RANGE - 0 to +50°C
THRESHOLD LINEARITY - ±0.25% Integral

TYPICAL CABLE LENGTHS (RG-58)
For Plastic, Nal and Si (S.B.) detectors- 0.5 to 1.0 m
For Planar Germanium detectors- 1.0 to 2.0 m
For Coaxial Ge- 2.0 to 4.0 m

TYPICAL POWER REQUIREMENTS
Standard version
+6 V - 150 mA, +12 V - 70 mA
- 6 V - 450 mA, -12 V - 100 mA

12V Version:
+12 V - 220 mA*
-12 V - 550 mA*

PHYSICAL
SIZE - Single width NIM module 3,43 X 22,12 cm (1.35 X 8.71 inches) per TID-20893 (rev.)
NET WEIGHT - 0.9 kg (2.0 lbs.)
SHIPPING WEIGHT - 2.2 kg (4.9 lbs.)
ACCESSORIES includeded:
Fraction module f = 0.4
Leading edge module
Zero cross module

Special version using ±12 V available on special request.
* This power exceeds the normal bin allotment of 167 mA for a singlewidth module for the 12V version

FAST ComTec GmbH
Grünwalder Weg 28A • 82041 Oberhaching • Germany
phone: 49-(0)89 665180 0 • fax: 49-(0)89 665180 40 • http://www.fastcomtec.com

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1. INTRODUCTION

1.1 GENERAL DESCRIPTION

* 100 MHz Countrate, 1000:1 dynamic range
* selectable fraction and program modules
* operating modes
  constant fraction CFT, slow rise time reject CFRR
  leading edge LET; zero-cross
* Walk less than $\pm$ 50 pS for 100:1 dynamic range, typical < $\pm$ 30 pS
* Positive and negative simultanous outputs
* Countrate indicating LED (green-orange-red)

The model CM 2128 is a fully DC-coupled constant fraction discriminator with a dynamic range of up to 1000:1. Selectable fraction and program modules and three operating modes provide optimum time resolution for many detector types and applications, for example

CFT constant fraction mode for fast detectors
CFRR slow risetime reject mode for Germanium detectors
LET leading edge mode for single photoncounting with a photomultiplier tube.

The model CM 2128 accepts negative polarity pulses to its 50 Ohm terminated DC-coupled input. The constant fraction composite signal is formed by the algebraic sum of a direct, attenuated signal path (ratio to 40 % by fraction module, changeable by user) and a delayed, unattenuated path. The delay time is user-selected according to the propagation delay of a cable connected between 2 front panel mounted BNC's. Optimum selection of this external delay provides full compensation of timing distortions due to both amplitude and rise time variations in the input signal.
Four simultaneous, independent output signals are provided. The two positive NIM voltage outputs are adjustable in width; the width duration sets the internal dead time as required to suppress spurious outputs due to input signal anomalies. The two independent negative NIM current outputs are derived as fixed-width pulses keyed to the start of the dead time period.

The wide dynamic range of the model CM 2128 permits its use in many applications without the need for fast pulse amplifiers. The front panel WALK ADJUST control permits the user to trim the time walk characteristic of the experimental set-up for optimum timing resolution.

1.2 SETUP INFORMATION

1.2.1 SELECTION OF PROGRAM MODULE

Module	Mode Switch	Comments
CF	CFT	Constant Fraction Discriminator
CF	CFRR	Constant Fraction Discriminator with slow rise time reject
CF	LET	Leading edge Discriminator, terminate Delay outputs with 50 Ohms Terminators
LE	LET	Leading edge Discriminator No termination needed for Delay outputs. The attenuated Input signal can be monitored on one of the delay connectors
Z/C	CFRR	Zero cross Discriminator No delay cable needed LE threshold must be crossed before zerocrossing of Input signal
Z/C	CFT	Zero cross Discriminator LE threshold can be crossed independent of zerocrossing of Input signal
Z/C	LET	2128 operates as leading edge Discriminator

1.2.2 SETUP INSTRUCTION FOR CONSTANT FRACTION MODE

For optimum time resolution of the CM 2128 follow these steps:

a) Set LET width as short as possible to cover the base of the Input signal
b) Set output width slightly longer than LET width

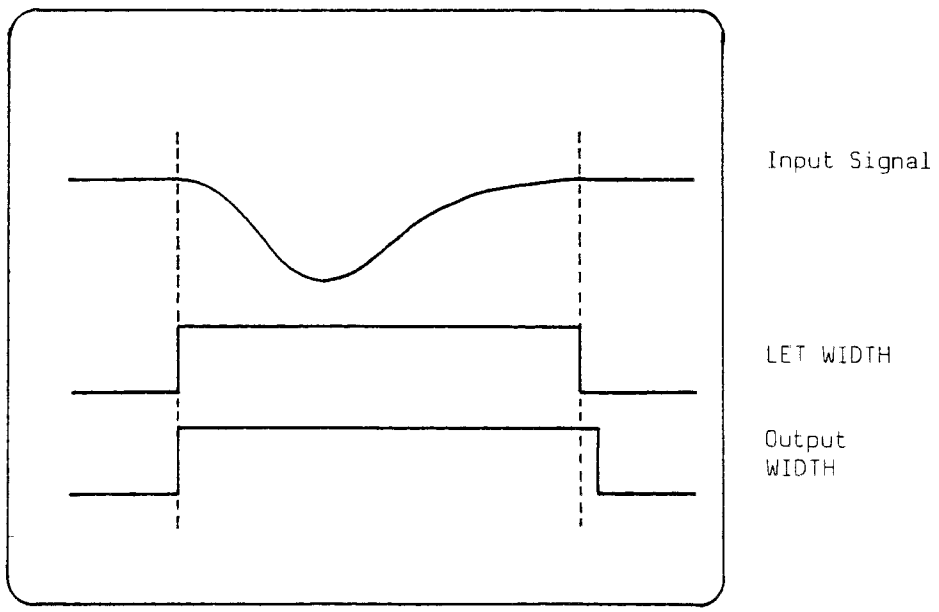


Fig. 1 Adjustment of LET WIDTH and Output WIDTH

c) adjust Inspect as shown

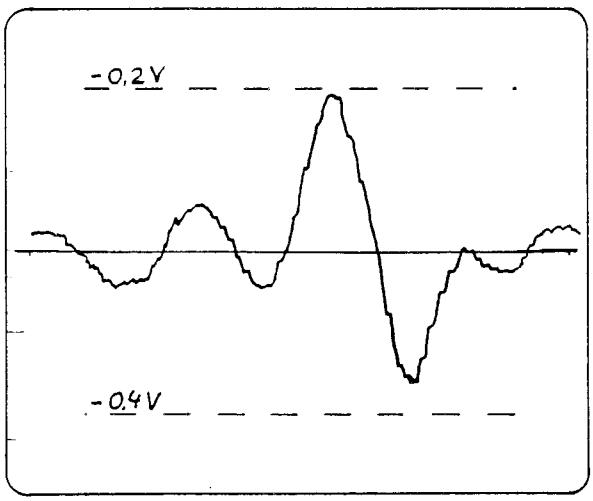


Fig. 2 - Avoid center setting

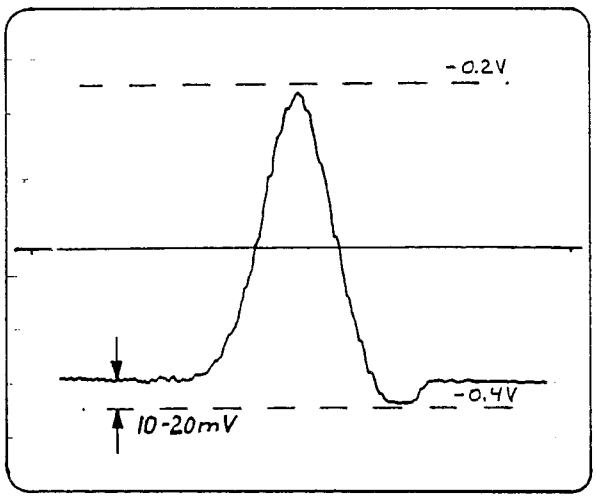


Fig. 3 A Correct off-center setting
for Plessey comparator SP 9687

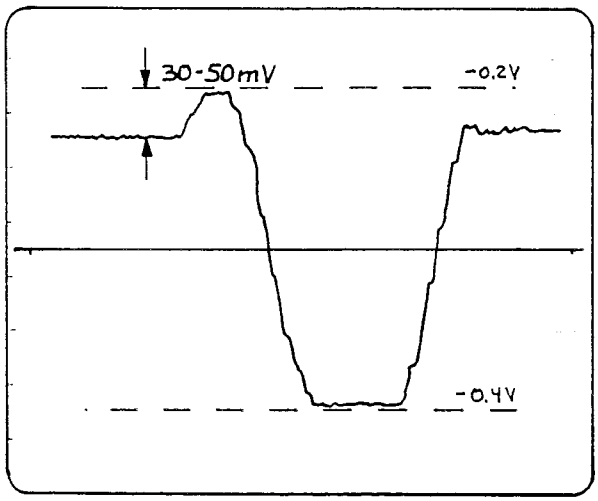


Fig. 3 B Correct off-center setting
for Advanced Micro Devices
Comparator AM 6687

Turn the level of the walk inspect signal down to lower baseline (dashed line as shown in Fig. 3 A), then adjust to 10 - 20 mV above baseline.
Symmetrical center setting should be avoided as the new ultra fast comparator SP 9687 (Plessey) deviates from its optimum time resolution in this setting.
If the SP 9687 is replaced by the new pin compatible comparator AM 6687 adjust as shown in Fig. 3 B.

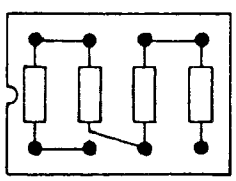
d) Remove Walk Inspect cable during measurement

e) CF Fraction module

If a different fraction is rquired change as follows:

Zo:f

Zo Zo Zo x f



CFT Module

Example fraction f = 0.2

Zo = 50 Ohms

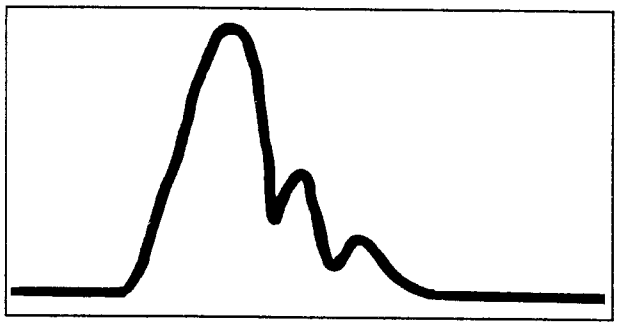
Zo x f = 250 Ohms (use 240)

Zo : f = 10 Ohms

Supplement to page 1b, Model 2128
November 1998

In new 2128 the double comparator has been replaced by two single comparators SP9680, VC9640 or MAX9685.

These comparators are pin compatible and show the same performance.



Setup:

Turn the level of the walk inspect signal down to the lower baseline.

Any setting around the center should be avoided as you will see an approx. 500 MHz oscillation only.

Your scope should be triggered with the fast output signal of the 2128. If an external clip cable is not installed (on rear panel BNC connectors) make sure the switch is set to the **internal** clip cable.

Do not terminate the inspect signal with 50 Ohms.

The shape of the inspect signal obviously depends on the input signal, the fraction and the delay line.

FAST ComTec GmbH · Grünwalder Weg 28a · D-82041 Oberhaching · Germany
Tel 49-(0)89-66 51 80 50 · FAX 49-(0)89-66 51 80 40 · http://www.fastcomtec.com

1.2.3 SETUP INSTRUCTIONS FOR LET MODE

a) Insert LET module for most convenient operation

b) Set the desired trigger level by adjusting the threshold potentiometer

c) Set LET width as shown in Fig. 1

c) Adjust output width as shown in Fig. 1

If CF module is used, terminate delay outputs with 50 Ohms terminators

1.2.4 SETUP INSTRUCTIONS FOR C/Z MODE

a) Insert C/Z module

b) Input signal must be bipolar negative lobe leading

c) Set mode switch to CFRR (optimum operation)

d) Adjust LET width wider than zero cross point of the input signal

If mode switch is set to CFT, LET does not have to overlap the zero cross point. This is useful if input signals with varying pulse width are used.

2. SPECIFICATIONS

2.1 INPUTS

INPUT

Accepts -5 mV to -5 V linear pulses
rise time in constant fraction modes
> 700 pS typically
Z_{in} = 50 Ohms, DC coupled
front panel BNC connector
minimum input pulse width > 1 nS
For LET mode the CM 2128 accepts shorter input pulses.

DELAY

2 BNC connectors between which a delay cable is connected to form the internal constant fraction signal.
Recommended lengths are based upon a cable propagation delay of ~1.5 nS/ft. (~5 nS/m) to provide a delay $0.2\ t_{rise}$ for Germanium detectors and ~$0.8\ t_{rise}$ for most other detector types ($1 - f \times t_{rise}$)

2.2 OUTPUTS

WALK INSPECT Displays output signal of zero crossing discriminator for use in trimming time walk.

LEADING EDGE Displays shaped leading edge discriminator output, width controlled by leading edge width adjust potentiometer

OUTPUTS (-) 2 independent negative current outputs, each providing - 32 mA into 50 Ohms, rise time ~2 nS,
pulse width 5 nS nominal, DC-coupled
The output signal width can be set to longer width by connecting an external cable between the two BNC connectors on the rear panel.
INT/EXT switch has to be set to EXT.

OUTPUTS (+) 2 independent positive voltage outputs providing 2 V (minimum) into 50 Ohms, rise time ~4 nS,
width adjustable by adjacent width trimming potentiometer, which also determines internal dead time

CLIP CABLE (REAR PANEL) 2 BNC connectors between which a delay cable is mated to clip the effective width of the negative output pulses, controlled by adjacent INT/EXT switch.

2.3 CONTROLS

THRESHOLD Front panel 10-turn locking dial potentiometer to set acceptance threshold for input pulses,
range -5 mV to -1 V.

WALK ADJUST Front panel trimming potentiometer to compensate walk of the internal zero crossing discriminator.

LEADING EDGE WIDTH 22-turn trimpot, adjusts width of leading edge discriminator pulse,used to overlap with negative going edge of walk inspect output

CFRR-CFT-LET	Front panel three position rotary switch to select constant fraction with slow rise time reject (CFRR), basic constant fraction timing (CFT) or leading edge timing (LET) modes of timing
WIDTH	Front panel 22-turn screwdriver adjust trimming potentiometer to set width of slow positive output pulse, which is equal to the internal dead time of the discriminator.
INTERN/EXTERN (REAR PANEL)	Toggle switch to permit cable clipping of width of negative outputs (EXT) or normal fixed width (INT)

2.4 INDICATORS

RATE	LED indicates activity of the discriminator Color of LED changes by count rate, between ~2 kHz and ~50 kHz green up to 5 kHz, orange 5 to 10 kHz, red above 10 kHz (for statistical input pulses)

2.5 PERFORMANCE

DYNAMIC RANGE	1000 : 1
WALK CFT MODE	In CFT mode (requires internal CFT module), for a 1 nS rise time pulse over a 100 : 1 dynamic range (reference -5 V), 50 pS. typically $\pm$ 30 pS
LEADING EDGE MODE	(requires internal LET module) Performance depends on rise time of input signal for 1 nS t_{rise} < $\pm$ 400 pS for a dynamic range of 10 : 1 500 pS for a dynamic range of 500 : 1
COUNTING RANGE	To 100 MHz, limited by dead time (WIDTH setting) (typically 120 MHz)
PULSE PAIR RESOLUTION	less than 10 nS or as limited by dead time
TRESHOLD STABILITY	Better than $\pm$ 0.02 %/°C ($\pm$ 200 ppm/°C)
TEMP. RANGE	0°C to + 50 °C
THRESHOLD LINEARITY	$\pm$ 25 % integral

2.6 TYPICAL CABLE LENGTHS (RG-58)

FOR PLASTIC, NaI and SI(S.B.)DET.	1.5 to 3.3 ft (0.5 to 1.0 meters)
FOR PLANAR GERMANIUM DET.	3.3 to 7 ft (1.0 to 2.0 meters)
FOR COAXIAL GE(LI)	7 to 14 ft (2.0 to 4.0 meters)

2.7 POWER REQUIREMENTS

STANDARD VERSION	+ 6V, 150 mA - 6V, 450 mA*
SPECIAL VERSION	+ 12V, 150 mA - 12V, 450 mA*

*) This power exceeds the normal BIN power allotment of 167 mA for a single width NIM module

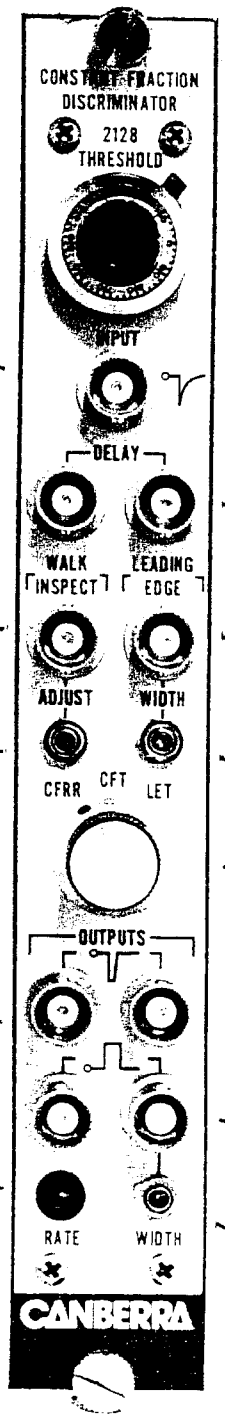
2.8 PHYSICAL

SIZE	Single width NIM module (1.35 x 8.71 inches) (3.43 x 22.13 cm) per TID-20893 (rev.)
NET WEIGHT	0.9 kg (2.0 lbs)
SHIPPING WEIGHT	1.8 kg (4.0 lbs)

3 CONTROLS, CONNECTORS AND INDICATORS

This section describes the functions of the controls, connectors and indicators of the CM 2128:

3.1 FRONT PANEL



Input accepts -5mV to -5 V linear pulses. Minimum input pulse width ~700 pS

Threshold sets threshold from -5mV to ~1V for signal acceptance

Delay for external delay cable used in CFRR and CFT modes

Walk inspect allows observation of zero crossing discriminator adjustment

Leading edge allows observation of leading edge output pulse width, has to overlap negative going edge of walk inspect pulse

Walk adjust varies the zero crossing timing in CFRR and CFT modes

L.E. width adjust leading edge inspect output width

CFRR - CFT - LET selects constant fraction with slow rise time reject (CFRR) constant fraction trigger (CFT) or leading edge mode (LET)

Negative output connectors each supplies -32 mV into 50 Ohms load

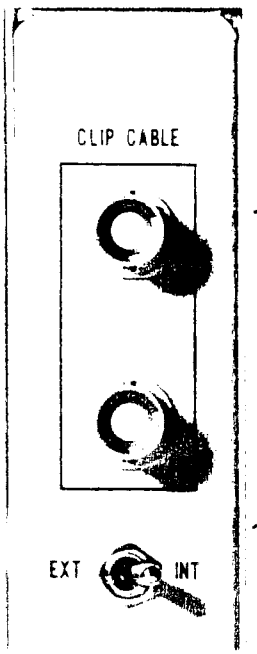
Positive output connectors each supplies a TTL logic signal into a 50 Ohms load

Rate LED indicates discriminiator count rate
green to ~5 kHz
orange ~5 to ~10 kHz
red above ~10 kHz (for statistical input pulses)
not calibrated!

Width control sets positive output signal width - also sets internal dead time

Fig. 4

3.2 REAR PANEL



Clip Cable negative output signal width clipping cable connectors

Internal: disables clipping

External enables clipping of negative output signal width

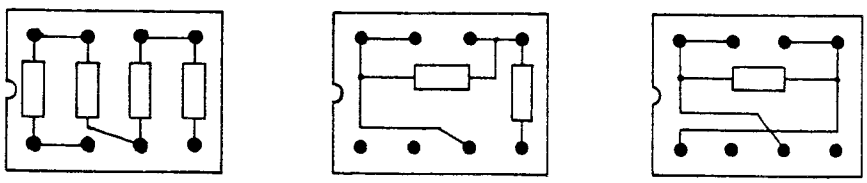
Fig. 5

INTERNAL CONTROLS

CFT MODULE Factory set to fraction f = 0.4 can easily be changed by customer see schematic diagram for details

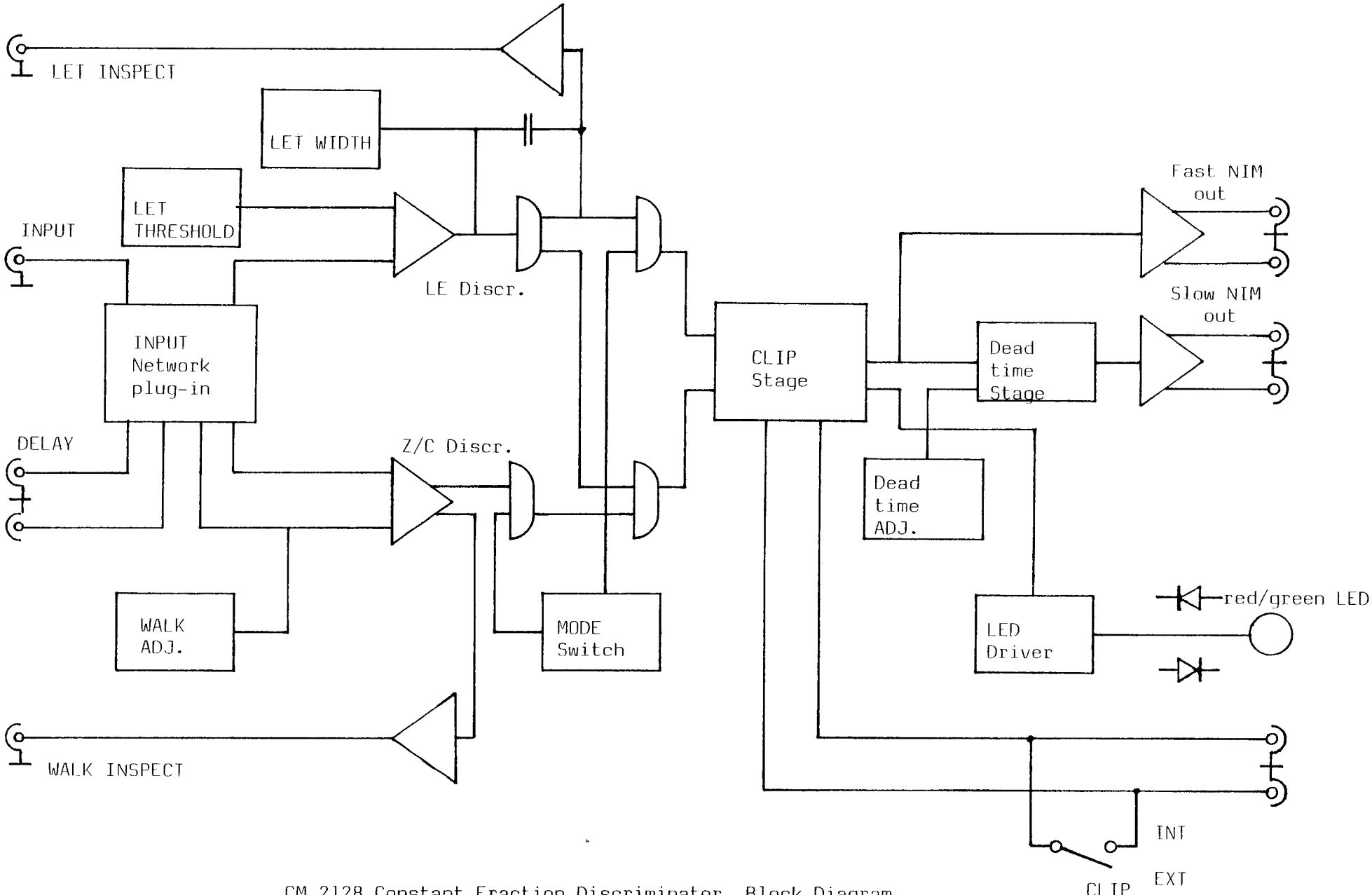
LET MODULE makes a LE discriminator out of the module - no termination of the delay BNC required

Z/C Module makes unit into zero cross discriminator, input signal must be bipolar, negative lobe leading)



CFT Module LET Module Z/C Module

Fig. 6



CM 2128 Constant Fraction Discriminator, Block Diagram

4 OPERATION

4.1 GENERAL

The purpose of this section is to familiarize the user with the operation of the model CM 2128 Constant Fraction Discriminator and to check that the unit is functioning correctly. Since it is difficult to determine the exact system configuration in which the module will be used, explicit operating instructions cannot be given. However, if the following procedures are carried out, the user will gain sufficient familiarity with this instrument to permit its proper use in the system at hand.

4.2 LABORATORY BENCH TESTS

Basic performance tests of the model CM 2128 may be exercised either in an equipment rack mounted BIN, or on a laboratory bench with the unit installed in, or powered by extender cable from a NIM BIN (TID-20893) (rev.). It is recommended that electrical connections be made with BIN power OFF.

4.2.1 INPUT

Suitable driving pulses may be obtained from laboratory pulsers or pulse generators (using the negative polarity outputs), or readily available detector pulse signals. Input signals should be limited to -5V peak amplitude.

4.2.2 OPERATING MODE

Selection of operating mode depends on the requirements of the given experiment. Some general compromises worth considering are given below:

In the leading edge mode (LET) the CM 2128 can be used as a 100 MHz leading edge discriminator by replacing the fraction module with the leading edge module. The mode selection switch is inoperative.
The leading edge mode should only be used with signals having a very short rise time and a very limited range of amplitudes as change in amplitude will cause walk.

In the Constant Fraction (CF) mode, timing is derived from a comparison between a fixed ration (40 % in the model CM 2128) and the peak amplitude of each successive pulse. This instantaneous self-reference yields a time mark that is theoretically independent of the pulse height, as contrasted to the behavior of the leading edge mode discussed above. In the model CM 2128 the ratio reference signal is taken internally, and the full amplitude pulse is delayed for the comparison using an external cable connected between 2 front panel connectors.

When the length of this external cable is chosen to generate a time delay less than the rise time of the input pulse, the resulting time mark is stabilized for both amplitude and rise time variations of that pulse. This is the basis for ARC (Amplitude and Rise time Compensated) timing. The compromise in Constant Fraction (and also ARC) timing is the ability to provide proper delays for the rise time of the input pulse considering

either rate and pile-up effects or the distortions introduced by varying wavefront shapes due to charge collection deficit, ballistic effects or trapping effects in the detector. It is these accomodations that lead to empirical determinations of the optimum delay cable length for a given detector and setup.

In the Constant Fraction with Slow Rise time reject (CFRR) mode, a further accommodation is offered for the longer rise times of solid state detectors. The timing mark for the Constant Fraction is derived from the slightly delayed pulse, with the presumption that the THRESHOLD level has been set quite low and this level is exceeded prior to the derivation of the timing mark. In the case of solid state detectors, where long varying wavefronts of the input pulse are common, a relatively short delay cable is frequently used and the above timing premise may not be satisfied. In that case, the amplitude discriminator keyed to the THRESHOLD setting may switch late, and the resulting timing will represent some mix of the intended Constant Fraction timing with Leading Edge timing. This effect causes tailing or a satellite peak in a time spectrum. In the CFRR mode, a logic alternation causes rejection of pulses which do not exceed the THRESHOLD prior to the derived Constant Fraction timing mark. The result is enhanced timing resolution due to elimination of the Leading Edge errors, but with some loss of counting efficiency.

4.2.3 DELAY CABLE

The delay cable used to set the Constant Fraction timing mark should provide a delay less than the known rise time of the applied input pulse for full compensation of both amplitude and rise time variations (for a fixed shape).
Generally the total delay required can be calculated by the following formula, where f = fraction and t_{rise} = rise time of Input signal (10 % to 90%)

$$t_{delay} \lesssim (1-f) \times t_{rise}$$

which was found to be the optimum for most applications.

The internal delay of the model CM 2128 is 0.3 nS, and this must be corrected in picking a suitable cable. For example, if the detector rise time is 5 nS, a 3 nS delay would be recommended. The external cable length, estimated on the basis of the 1.46 nS per foot for RG-58 cable, would be:

$$L = \frac{\text{External Delay}}{1.46} = \frac{\text{Total delay - Internal Delay}}{1.46}$$

$$L = \frac{3.0 - 0.3 \text{ nS}}{1.46 \text{nS/ft}} = 1.85 \text{ ft or about 22 inches (56 cm)}$$

For very short pulses ($t_{rise} \lesssim 2$nS) we recommend to measure the delay direct at the high speed comparator. (Pin 7 and Pin 8) and to directly install the necessary delay cable without the front panel BNC's.

4.2.4 WALK TRIM

The adjustment of the amplitude sensitive variation of the timing mark (time walk) in the Constant Fraction and CFRR modes remains a less exact procedure. Proper adjustment is possible only when the D.C. offset present on the input to the model CM 2128 is less than ± 6 mVDC. Thus detector leakage or dark current errors must be minimized before attempting adjustment

Laboratory trimming of the unit can be demonstrated by using a suitable pulse generator with a known fast, clean wavefront and a delay chosen as discussed above. A very broadband 50 Ohm attenuator such as the Hewlett Packard HP-3496, or one whose time walk is very precisely known, should be used. An externally triggered oscilloscope capable of displaying at least 1 nS/division is also necessary. Step attenuations should be then yield a stable time position of the output signal of the model CM 2128, when starting from a reference -5 V peak pulse input. Care must be taken that the pulse generator offset is small and does not change for different attenuator settings. The WALK ADJUSTMENT trimming potentiometer can be used to find the best adjustment of the finite time walk over a narrower amplitude range as desired.

When the model CM 2128 is used with the intended detector, timing resolution may be trimmed experimentally by successive measurements in the setup at hand, because the timing resolution depends on many parameters such as the fraction, threshold, delay cable and walk inspect setting used. A qualitative monitoring is available by monitoring the front panel INSPECT output with an oscilloscpe. For fast detectors the output should appear between -0.2 V and -0,4 V (use DC-coupling of scope for convenient display) and should look as shown in Fig. 7.
For slower detectors, a noise band between the levels may be seen, with transitions to high and low of about equal intensity. Reference Fig. 8.

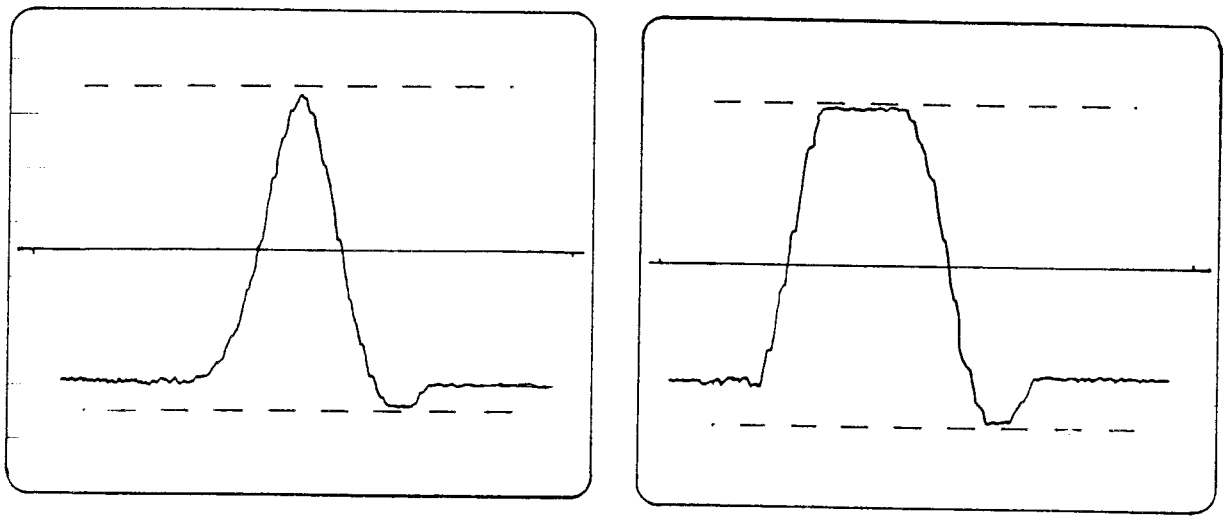


Fig. 7 Walk Inspect wave forms
using Plastic Detector

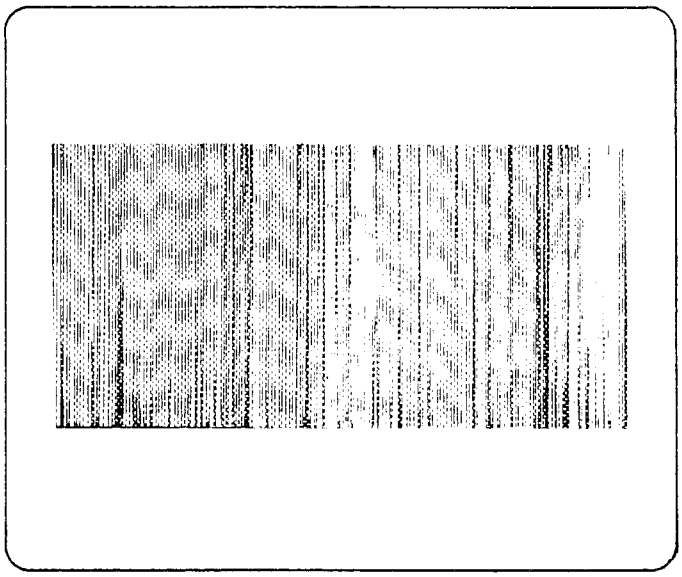


Fig. 8 Walk inspect wave form
for Slow Detectors

4.2.5 OUTPUTS

The output logic pulses from the model CM 2128 are intended to drive 50 Ohm loads through any reasonable length of suitable 50 Ohm coaxial cable (such as RG - 58). Fig. 9 shows the typical output pulse shapes into 50 Ohm loads, with the WIDTH control set to minimum.

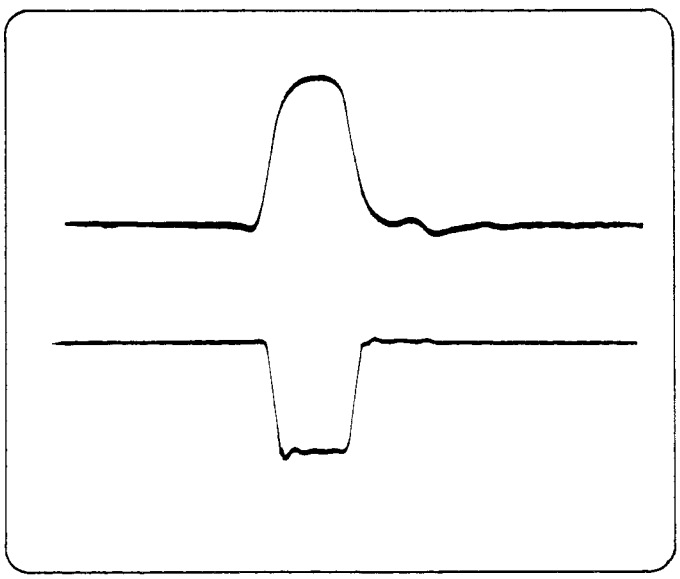


Fig. 9 Typical output pulses into
50 Ohms load
lower trace: 0.5 V/division,
5 nS/division

Since the WIDTH control also sets the DEAD TIME following a given pulse, the user should set this control consistent with the pulse rate requirements of the given experiment. In the minimum (fully counter-clockwise) position of the WIDTH control, a count rate in excess of 100 MHz can be expected in each mode of the model CM 2128.

4.2.6 CLIP CABLE

The clipping cable function on the rear panel allows the user to set the width of the negative NIM current outputs as desired by applying a suitable delay cable between the BNC connectors and setting the adjacent toggle switch to EXT. If the toggle switch is left in the INT position, the negative pulse width will be ~4 nS (nominal)

5. Circuit Description

5.1 General Description

The model CM 2128 provides the advantages that various modes to derive the timing signal can be chosen by changing either the input network plug-in (CFT, LE, Z/C) and/or by selecting the desired mode (CFRR, CFT, LET) by the frontpanel mode switch. This model utilizes a direct coupled negative input to perform integral discrimination or/(and) to derive a constant fraction timing mark. The bulk of the logic signal processing is executed in emitter-coupled integrated circuit logic (ECL). Since the circuitry can operate in various modes, its operation is best appreciated by understanding the simplest mode (LET), and then adding the provisions for the other ones.

5.2 Leading Edge Mode (LET)

In this mode (see details for either plug-in or mode switch) the model CM 2128 acts as a simple integral threshold discriminator. In this mode, both pulse amplitude discrimination and timing are derived in A 1 (see circuit diagram). The pulse acceptance level is established by the frontpanel threshold potentiometer, which is set for a range of -5 mV dc (nominal) to -1.0 V dc. Since the timing mark for the comparator A 1 (1/2 of SP9687) is derived from the point where the pulse wavefront intercepts the threshold setting, it is quite obvious that the timing mark changes with amplitude and risetime of the input pulse.
The comparator A1 provides an ECL logic pulse (-1.7 V to -0.4 V) at its PIN 16. This signal is accepted through gate G1 (1/4 of 10H102) appearing at the output Pin 9 as a positive going signal (-1.6 V to -0.8 V) and at the output PIN 15 as a negative going signal (-0.8 V to -1.6 V). The width of these signals depends on the setting of the leading edge width potentiometer (frontpanel L.E. width adjust). The width of the signal can be monitored at the frontpanel BNC connector LEADING EDGE. The negative going ECL output signal of G1 is accepted through gate G4. Note that with the setting of the frontpanel mode switch to L.E. the output of the gates G2 (PIN 3) and G3 (PIN 14) is always set to logic LOW (-1,6 V). The output of gate G4 is fed to the clock enable input (PIN 6) of a master-slave type D flip-flop (1/2 of 10H131). The Q-output (PIN 2) is fed to a bus driver (10192) and converting the ECL levels to fast NIM levels (- 32 mA to 50 Ohm outputs). The width of the output pulse is determined by the CLIP cable connected to set S (PIN 5) and Q (PIN 3) of the flip-flop. The output of Q goes to the clock enable input (PIN 11) of the second master-slave type D flip-flop (second half of 10H131). The Q output (PIN 15) is converted by the following ECL-to-TTL translator (10H125) to a positive TTL output pulse. The width of the positive output signal is set by the frontpanel potentiometer (WIDTH control). This width also determines the internal deadtime of the module.

5.3 CONSTANT FRACTION MODE (CFT) and CONSTANT FRACTION SLOW RISETIME REJECT MODE (CFRR)

In the normal constant fraction mode the applied input signal is sensed for amplitude by A1 as above, but also routed to the frontpanel DELAY cable BNC connector (see section 4.2.3). The delayed pulse is applied to the inverting input (PIN 7) of A2. (1/2 of a ultra fast dual comparator SP9687 or AM 6687)

The prompt but attenuated signal (attenuation determined by the fraction module) is applied to the non-inverting (complementary) input (PIN 8) of A2. The difference signal between these inputs is algebraically a bipolar pulse whose zero crossing is the time mark. Time walk for the bipolar signal is theorectically zero.Finite errors, such as a small dc offset on the input, the offset bias of the comparator, as well as the finite gain-bandwidth of the device cause some time shift or walk in actual case. With the front panel Walk Adjust - by monitoring the Inspect signal - (one output of the comparator) one has the possibility to minimise the time walk.
The WALK INSPECT connector (output on PIN 2 of A2) provides an indication of A2's switching. For setting of the WALK INSPECT see section 4.2.4
The logic output of A2 (PIN 1) is applied to gate G2 (PIN 7). Note switch A is not grounded in CFT operation. The outputs of G2 (PIN 3) and G1 (PIN 15) are applied to gate G4. In normal operation the first negative going pulse is provided from gate G1. The following pulse logic is identical to that as described in section 5.2 Note that in CFT operation switch B is grounded - the level at the D input (PIN 7) of the flip-flop is always logic LOW (-1.6 V)

To resolve those conditions where slower rise time pulses (such as those degraded by charge trapping or incomplete absorption, for instance) may cause poor timing performance, the CFRR mode locks out and rejects those pulses which do not satisfy the THRESHOLD setting prior to the derived constant fraction mark.This inadvertent timing marks derived from the leading edge discriminator A1 switching late are blocked.
In the CFRR mode switch B is left open. The output signal gate G1 (PIN 9) is processed through gate G3. The negative going output signal (-0.8 V to -1.6 V on PIN 14) of the gate G3 is applied to the data (D) input (PIN 7) of the flip-flop (1/2 10H131). Therefore output signals are only generated when the threshold signal (A1) is prior to the derived constant fraction timing of A2. Inadvertent timing marks derived from the leading edge discriminator switching late are blocked.

5.4 Z/C

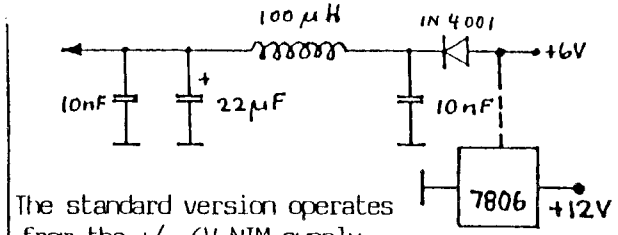
For this mode (input network plug-in) a bipolar input signal (negative leading lobe) is necessary. The timing mark is derived from the zero crossing of the bipolar signal. For details in setting the LET width (monitored at the LET Inspect) see details in the manual.

Switch position

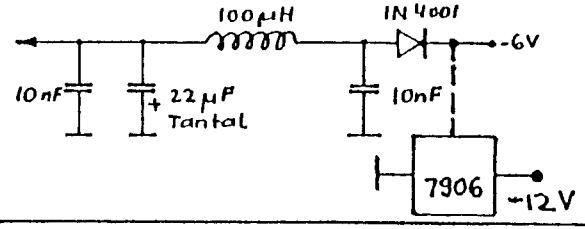
	A	B
CFRR	open	open
CFT	open	ground
LET	ground	ground

CF Fraction Plug-in

factory set to f = 0.4
Zo = 50 Ohms
Zo:f
Zo x f
can easily be customer modified



The standard version operates from the +/- 6V NIM supply
For the special version voltage regulators are added (dashed line)

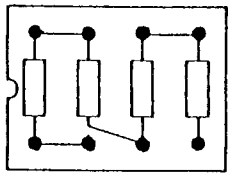


Plug-in for:

CF (Fraction 0.4 standard)

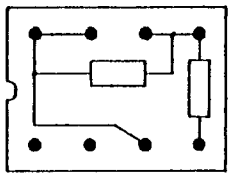
Zo:f

Zo Zo Zo x f



CFT Module

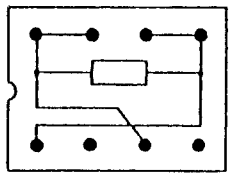
Zo



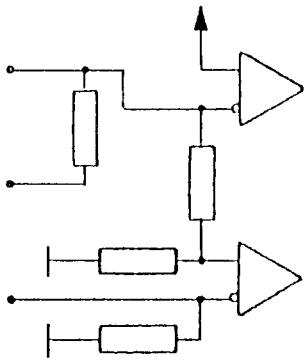
10 Zo

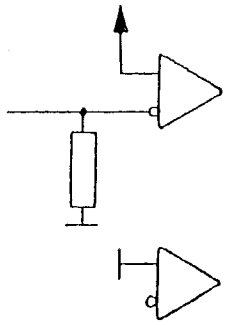
LET Module

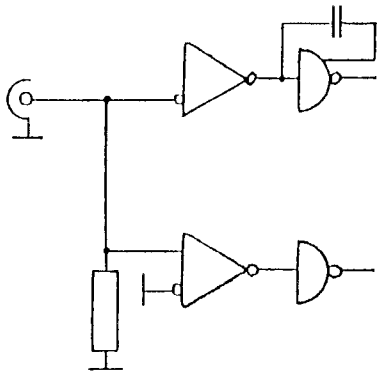
Zo



Z/C Module







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